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Moving Towards Two-Phase Micro-Cooling of 3D Integrated Circuits

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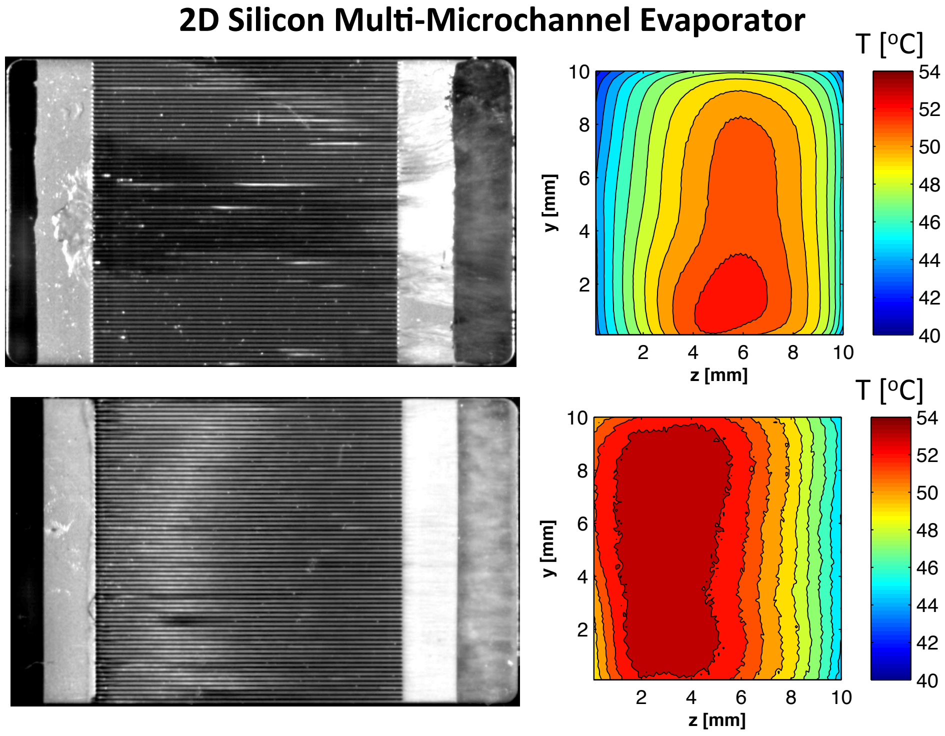
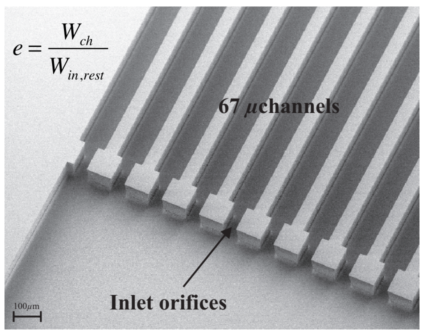
Motivation

3D IC stacked architectures with interlayer cooling offer an excellent opportunity to continue the CMOS performance trends over the next decades. The difficulties and costs in designing and fabricating such 3D systems do not allow sufficient devices to be tested in order to determine their optimal geometries and operation. Therefore, there is a need to accurately measure the performance of the individual layers beforehand.

2D Silicon Multi-Microchannel Evaporator



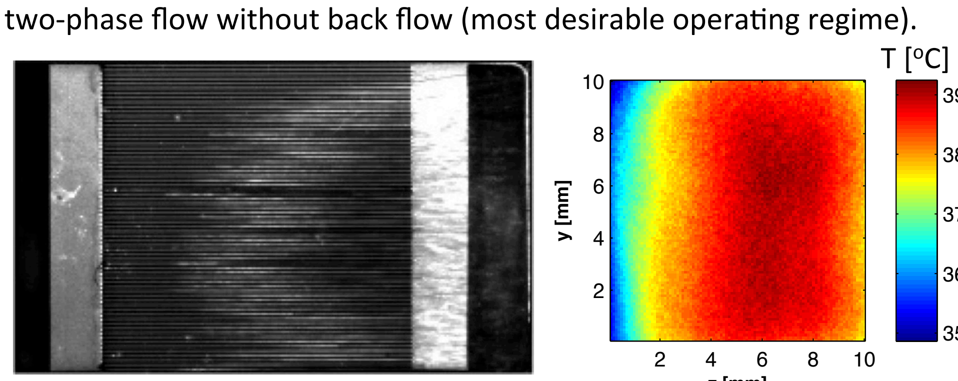
Snapshots of the high-speed flow visualization and the time-averaged IR temperature maps provided by the two-phase flow boiling of R245fa in the test section without any inlet restrictions (top line), and with the 50 μm-wide, 100 μm-deep, and 100 μm-long inlet micro-orifices (bottom line). The flow is from left to right in all the presented images. G_{ch}=2'035 kg/m²s and q_b=36.5 W/cm².



Significant flow instabilities, vapor back flow, and non-uniformity of the flow among the channels were observed in the test section without any inlet restrictions. In order to prevent these phenomena, 100, 75, 50, 25 μm-wide, 100 μm-long, and 100 μm-deep inlet restrictions were successfully utilized.

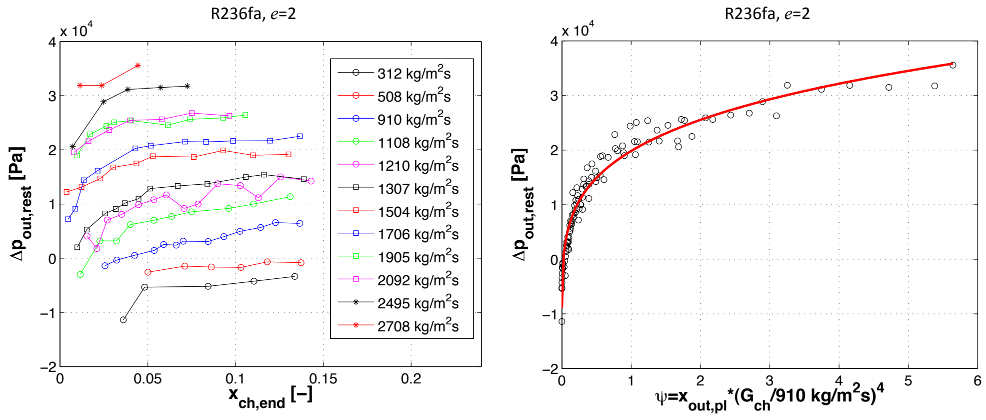
Experiments

Eight different operating regimes of the two-phase flow boiling of R245fa, R236fa and R1234ze(E) in the micro-evaporator with the inlet restrictions were distinguished: (1) single-phase flow in the test section with the vapor bubbles at the outlet manifold's plenum, (2) single-phase flow followed by two-phase flow with back flow, (3) unstable two-phase flow with back flow developing into jet flow, (4) jet flow, (5) single-phase flow followed by two-phase flow without back flow (presented below), (6) two-phase flow with back flow triggered by bubbles formed in the flow loop before the test section, (7) flashing two-phase flow with back flow, and (8) flashing two-phase flow without back flow (most desirable operating regime).



Snapshot of the high-speed flow visualization and the time-averaged IR temperature map of the test section's base provided by the two-phase flow boiling of R236fa in the multi-microchannel evaporator for G_{ch}=1'299 kg/m²s, q_b=13.5 W/cm².

Outlet Restriction Pressure Drop

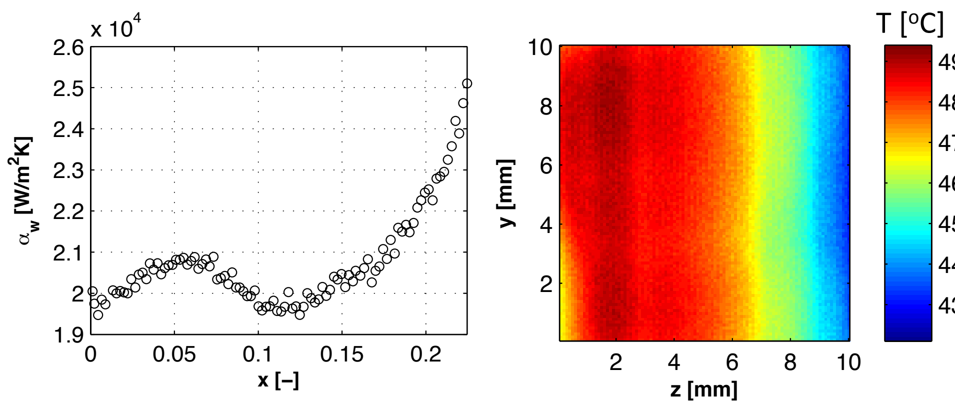


The outlet restriction pressure drop is correlated based on the outlet plenum conditions. For R236fa and the expansion ratio of *e*=2:

$$\Delta p_{out,rest}(\psi) = 35441\psi^{0.21532} - 15607$$

where: $\psi = x_{out,pl}\left(G_{ch}/910\,\mathrm{kg/m^2s}\right)^4$

Two-Phase Heat Transfer Coefficient



The lateral-averaged wall heat transfer coefficient provided by the two-phase flow of R236fa in the test section with the 50 μm-wide 100 μm-long, and 100 μm-deep inlet restrictions, thus *e*=2, for G_{ch}=2'299 kg/m²s, q_b=48.6 W/cm² as a function of local vapor quality.

Conclusions

- The inlet micro-orifices are required in order to prolong the lifetime of future 3D interlayer cooling systems and to extend their stable operation.
- In addition to the two-phase flow pattern, the overall stability of refrigerant flows in multi-microchannel evaporator was investigated and eight different operating regimes were distinguished. The flashing two-phase flow without back flow was found to provide the best flow and thermal stabilities.
- The outlet restriction pressure drop due to the complex geometry is correlated based on the outlet conditions measured within the outlet manifold's plenum.

References

1. S. Szczukiewicz, N. Borhani, J. R. Thome, *Experimental Investigation of Diabatic Flow in Microchannels using Infra-red Thermography*, September 2010, XIV Heat and Mass Transfer Symposium, Poland.
2. M. M. Sabry, A. Sridhar, D. Atienza, Y. Temiz, Y. Leblebici, S. Szczukiewicz, N. Borhani, J. R. Thome, T. Brunschwiler, B. Michel, *Towards Thermally-Aware Design of 3D MPSoCs with Inter-Tier* Cooling, March 2011, Design, Automation, and Test in Europe Conference, France.
3. S. Szczukiewicz, N. Borhani, J. R. Thome, *Two-Phase Flow Boiling in a Single Layer of Future High-Performance 3D Stacked Computer* Chips, May 2012, ITherm2012: 13th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, USA.
4. S. Szczukiewicz, N. Borhani, J. R. Thome, *Two-Phase Heat Transfer and High-Speed Visualization of Refrigerant Flows in 100 x 100 µm² Silicon Multi-Microchannels*, June 2012, ECI 8th International Conference on Boiling and Condensation Heat Transfer, Switzerland.

Acknowledgements

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