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# Integrated Water Cooled 3D Electronic Chips: Modeling and Experiments

**CMOSAIC** 

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**Modeling** - A novel, non-equilibrium porous medium based model is used to predict high local thermal gradients in vertically integrated (3D) chip stacks. The cooling structures are simulated as ultra thin porous medium with orthotropic thermal conductivity and variable thermophysical properties. Moreover, we specifically account for the hydro-thermal entrance region.

**Experiments** – Hydrodynamics and heat transfer in microcavities with micropin fin arrays, simulating through-silicon-vias, is investigated. High through put, transition flows are characterized through dynamic pressure and flow visualization. Vortex shedding and flow impingement onto the pins enhance the mass transfer and a higher heat transfer is expected.



inside the chip after the hydrodynamic transition. The shedding frequency increases linearly for higher Re

## Visualization of Flow Fluctuations

Illuminated particle pathlines

**Optical estimation of the frequency** 

a) Post-transition pathlines showing enhanced mass transfer

flow



b) Incomplete flow cycle with an exposure time of **t<sub>exp</sub>=100 μs** shows the upper frequency limit

pressure signal  $f_{meas} \sim 6.3 \text{ kHz}$ 

# 3D Chip Stack Model

 $C \operatorname{Re}^{\alpha} \operatorname{Pr}^{\beta}$ 

**RTD 2009** 

Computationally efficient non-equilibrium porous medium model specifically accounting for the hydro-thermal entrance region



a) Schematic slice of the chip stack model



0.4 <sub>×\*</sub> 0.6

temperatures

c) Validation of junction and hot-spot

▲ ▲ Top

0.8

Temperature 306 2-port chip stack 303 300 296 293 [K]

, for X or  $X_T < x < L$ 

FNSNF

b) Temperature distribution in a 3D chip stack modeled as porous medium



field of view 1.2 mm



c) With **t**<sub>exp</sub>=200 µs, the repetitive shedding cycle shows that 5 kHz < f<sub>shed</sub> < 10 kHz

### Future Work

#### **Experiments:**

Heat transfer: measurement of water and micro pin-fin temperatures in the vortex shedding regime
Integrate novel results in an improved 3D chip stack

#### Modeling:

- Transient modeling: vortex shedding

Temper

- Impact on the performance of non-homogeneous micro pin-fin density and heat fluxes

0.2



d) Pin-Fin structures are better in cooling than microchannels

#### Publications:

Alfieri et al., 3D Integrated Water Cooling of a Composite Multilayer Stack of Chips, J Heat Trans (2010)

Alfieri et al., On the Significance of Developing Boundary Layers in Integrated Water Cooled 3D Chip Stacks, Int J Heat Mass Tran, accepted for publication (2012)

Renfer et al., Experimental Investigation into Vortex Structure and Pressure Drop Across Microcavities in 3D Integrated Electronics, Exp. Fluids (2011)

Renfer et al., Vortex Shedding from Confined Micropin Fin Arrays, Microfluidics and Nanofluidics, to be submitted (2012)



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