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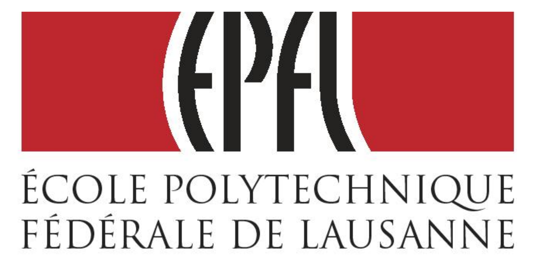
Wafer-Level Deep TSV Process for 3D Integration



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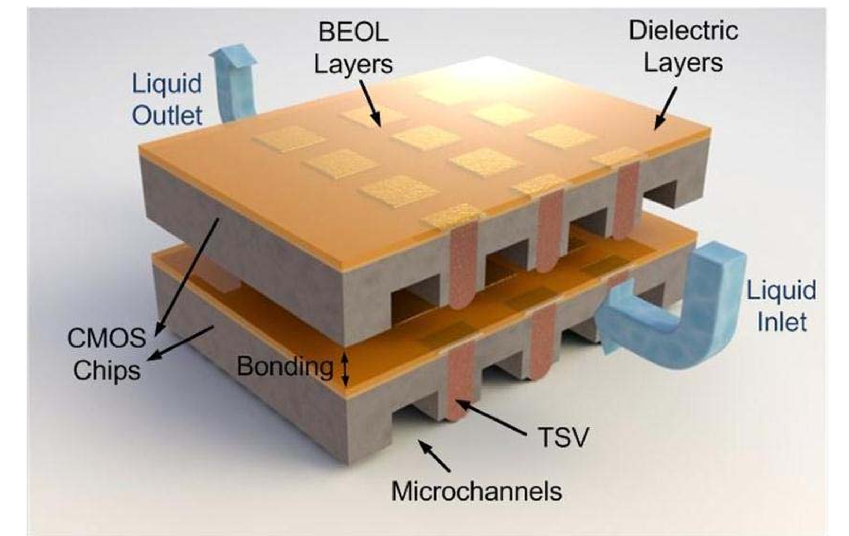
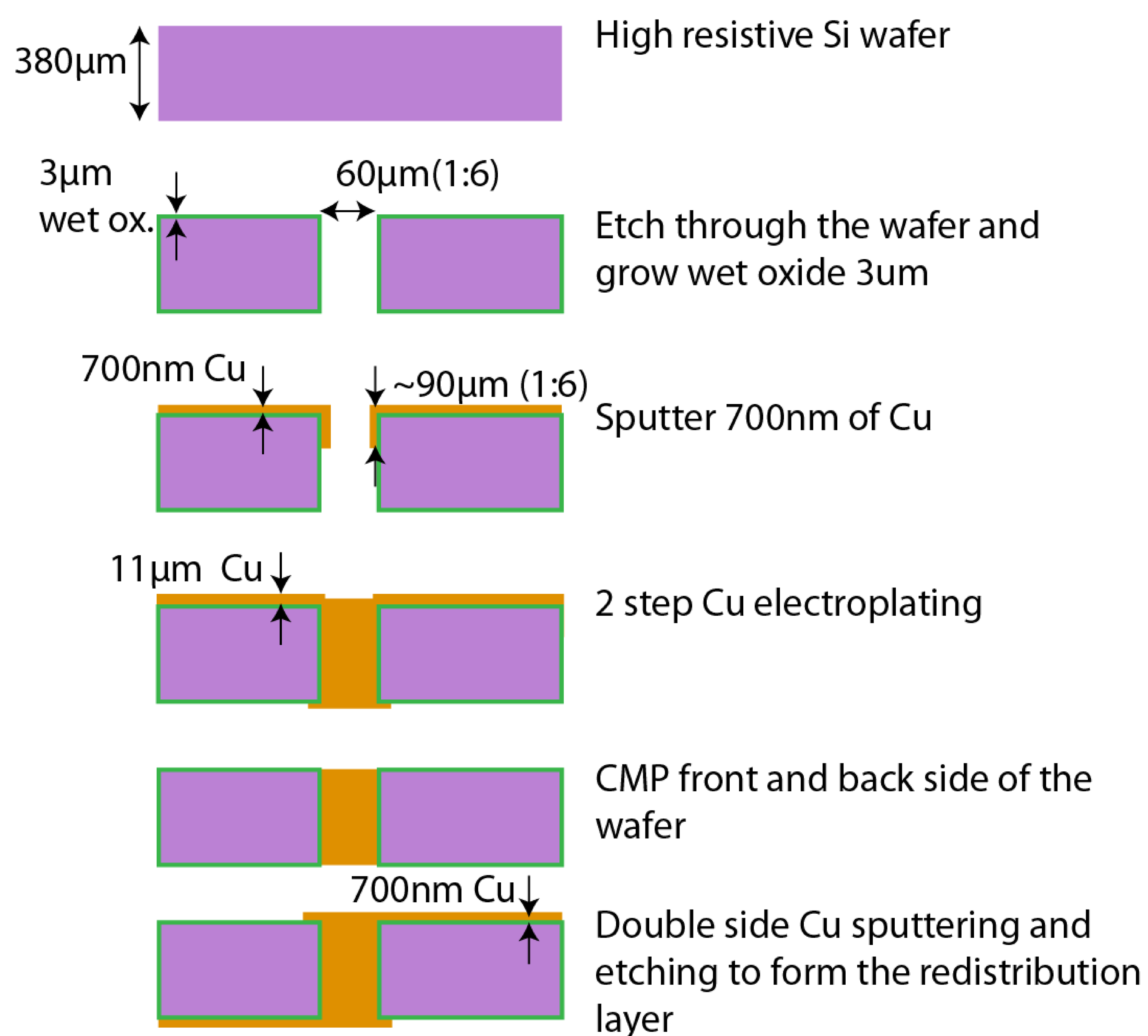
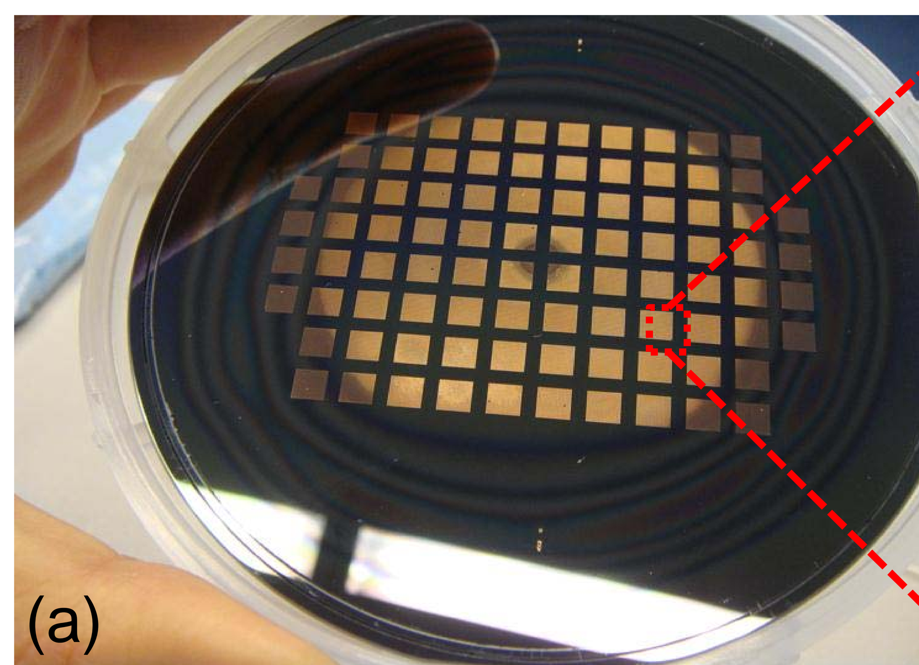
INTRODUCTION

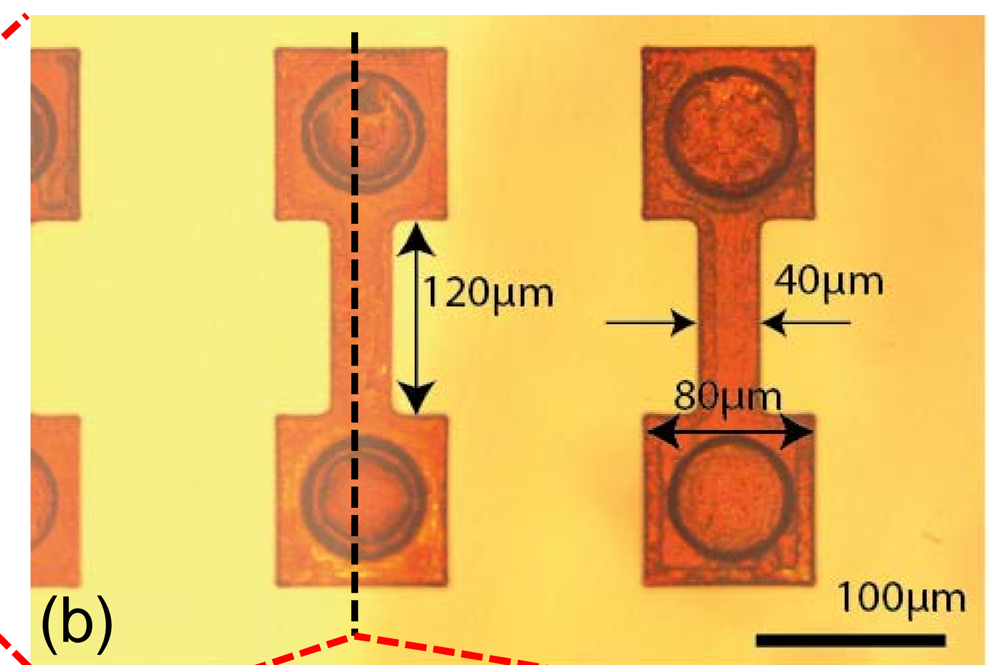
This poster reports a new processing platform for wafer-level through-silicon-via (TSV) fabrication, based on single wafer bottom-up Cu electroplating. The goal of this work is to develop a TSV fabrication and 3D integration platform for the applications requiring thick Si substrates with deep and fully-filled TSVs. The technique enables the processing of frontside micro-heaters and backside micro-channels for liquid cooling experiments. TSVs with aspect-ratios higher than 6:1 are demonstrated and characterized through resistance and capacitance measurements. ***Zervas et al., ECTC'12***

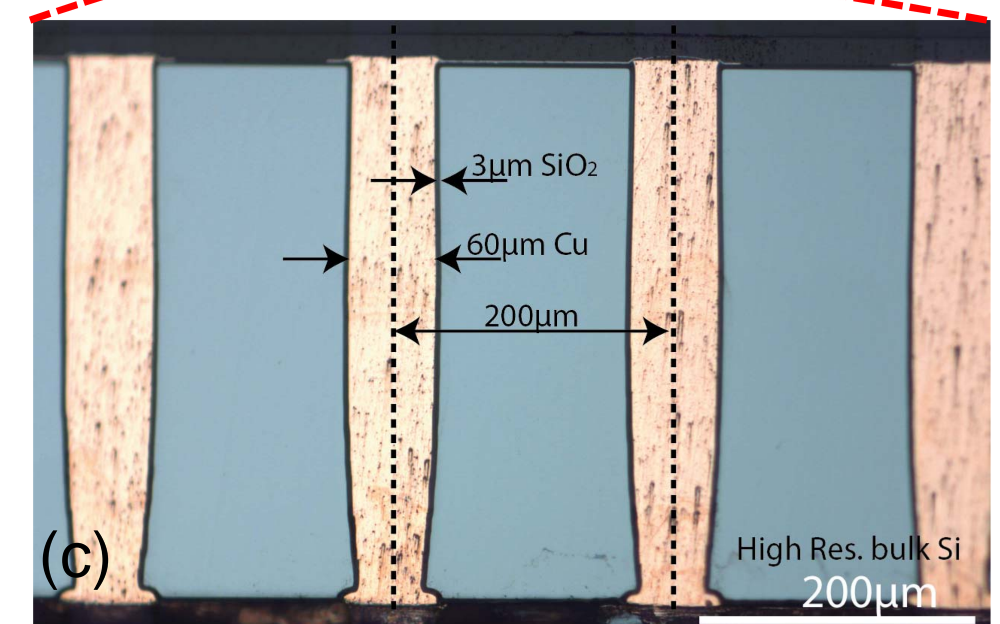


Fabrication



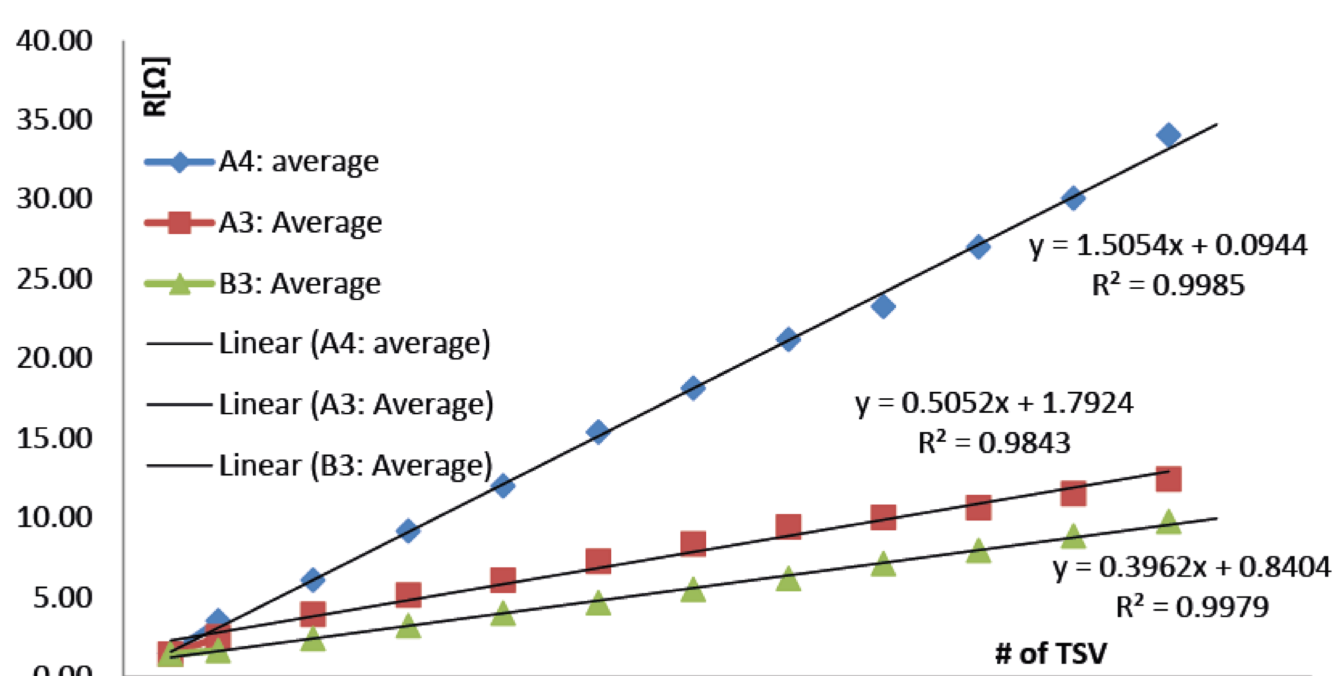


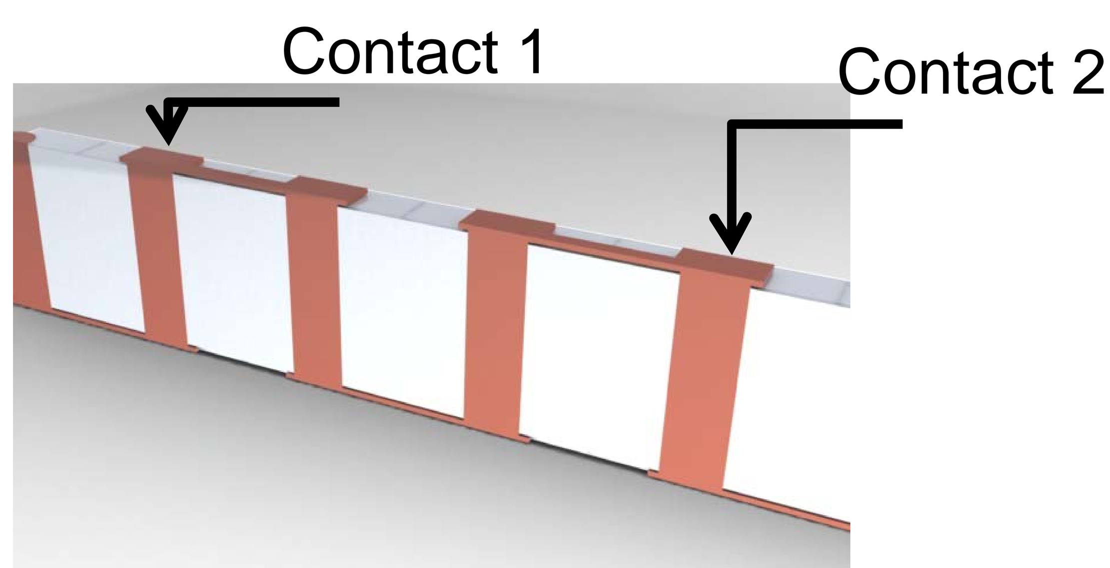


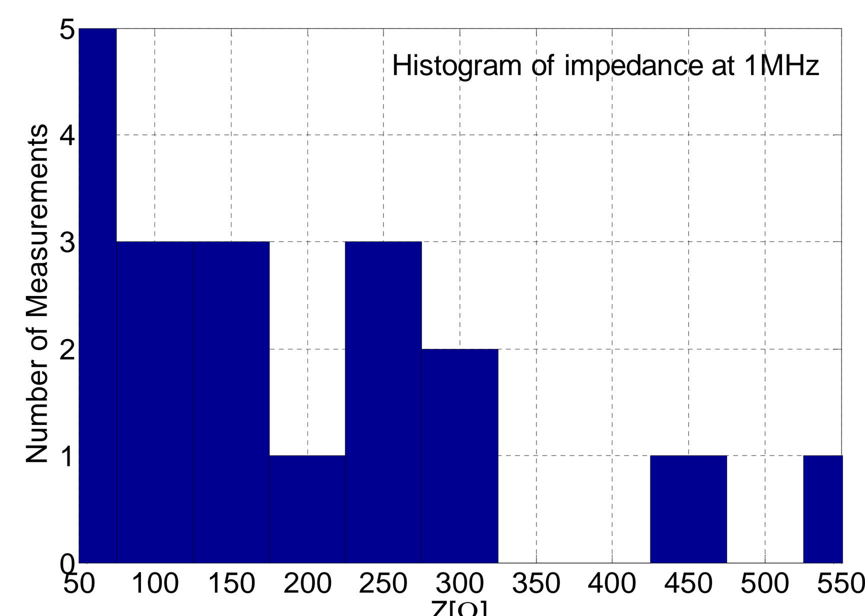


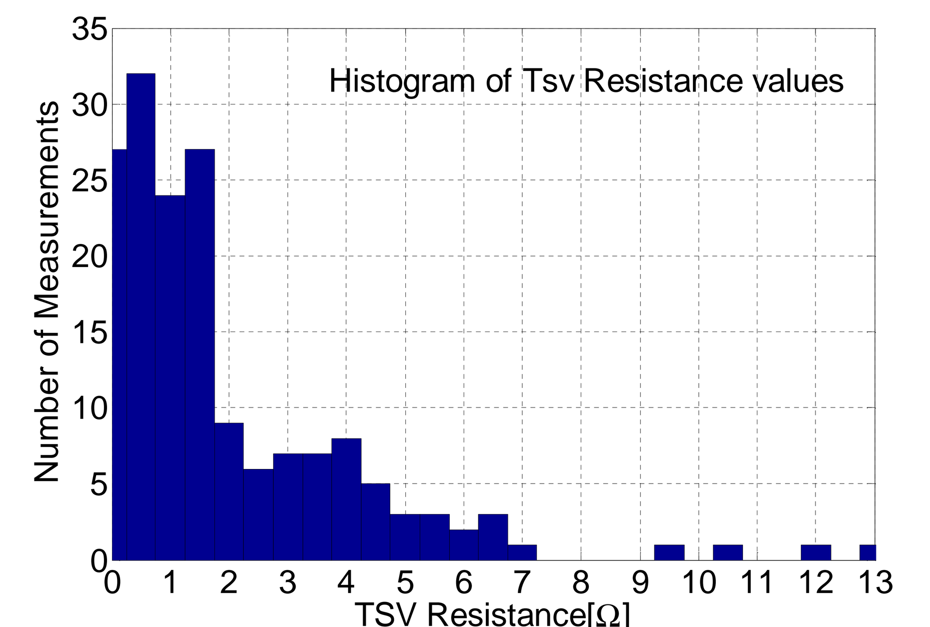
Process flow (left side) and fabricated devices (right side). Wafer with TSV test chips (a). The TSVs are grouped into clusters of 900 and connected to daisy chain configuration. Top view (b) and cross-section view (c) of the fabricated daisy chain patterns.

Measurement Results









Daisy-chain measurements

- **900 TSVs** serially connected in a single daisy-chain configuration.
- Resistance per TSV: **0.7 Ω**
- Capacitance per TSV: **0.8 pF**
- Maximum current before failure: **1.7A**
- Thermal testing up to **300 ºC**