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# Enabling energy efficient tunnel FET-CMOS co-design by compact modeling and simulation


*R. Rhyner[1], C. Bessire[2], L. De Michielis[3], N. Dağtekin[3], A. Biswas[3], A. Schenk[1], M. Bjoerk[2], K. Moselund[2], H. Schmid[2], H. Riel[2] and A. M. Ionescu[3]*

[1]: Integrated Systems Laboratory, ETH Zurich; [2]: IBM Research – Zurich; [3]: STI-IEL-Nanolab, EPF Lausanne


This project is addressing the power dissipation as the greatest challenge for today's nanoelectronics. Tunnel-FETs are steep slope switches that target critical power issues and are considered in research and industry as the candidate with the highest potential for low power circuits and systems. To achieve its full potential it is required to understand the device physics, optimize its performance and be able to establish the modeling and simulation environment necessary to enable the co-design of steep slope switches with advanced CMOS for novel energy efficient integrated circuits.

## ETHZ

Modeling of transport in bulk-like Si tunneling diodes, the basic elements of corresponding tunneling FETs, needs to include electron phonon interaction. Combining electron phonon scattering and an atomistic full-band basis, as needed in nanoscale device simulations, is a real challenge from a computational and theoretical point of view [1, 2]. We present here a first validation of electron phonon interaction in an atomistic full-band basis for bulk-like structures by means of simulations of phonon-assisted band-to-band tunneling currents in Esaki diodes.

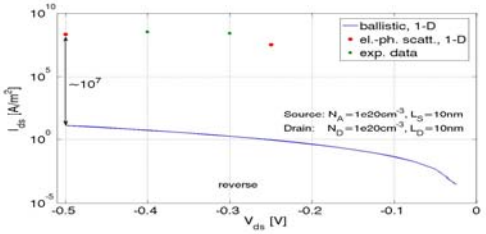


Fig. 1: Comparison of the ballistic Ids − Vds curve of a 1-D structure against two points calculated with full electron-phonon interaction and experimental data[3].

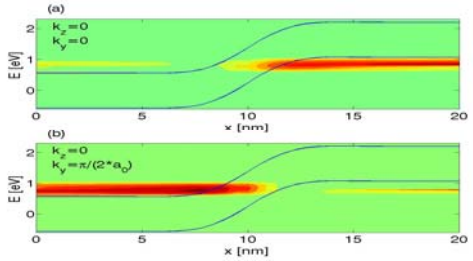


Fig. 2: Energy- and position-resolved dissipative current for the 1-D structure (Fig. 1) at Vds = −0.5V . Dark red indicates high current concentrations, light green no current. The blue lines show the band edges. (a) and (b) represents two different (ky, kz) combinations.

## IBM

Si-InAs nanowire Esaki diodes have been fabricated and characterized [4]. The influence of interface traps is investigated.

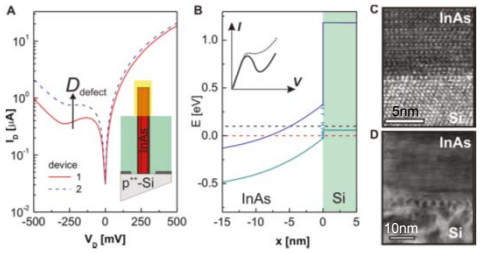


**Fig. 3:** Defects in tunnel diodes. (A) IV characteristics of two Si-InAs heterojunction tunnel diodes. The spread in current in forward bias arises from different levels of excess current. (B) Calculated band structure of the Si-InAs heterostructure under 100mV forward bias. (C) High-resolution transmission electron micrograph of the Si-InAs interface. (D) Tilted view of the interface showing the dislocation network at the interface.

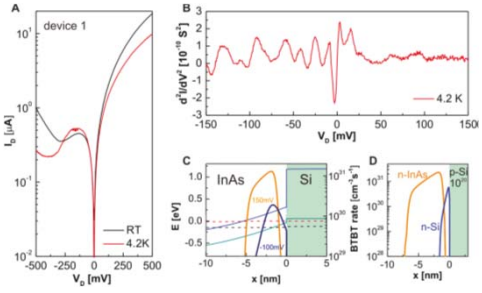


Fig. 4: (A) Comparison of IV characteristics of a Si-InAs tunnel diode at room temperature and 4.2 K. (B) The second derivative of current with respect to the voltage at 4.2 K exhibits pronounced peaks in forward bias originating from trap-assisted tunneling due to defect states in the bandgap. (C) Calculated band diagram (at 300 K) of the Si-InAs junction at 150 mV reverse bias. (D) Comparison of the calculated BTBT rates (at 300 K) for the Si-InAs tunnel heterostructure diode as used in the experiments.

### REFERENCES


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## EPFL

A Band-to-Band tunneling analytical model for reverse biased homo- and hetero- p-n junctions has been developed, validated by means of numerical simulation [6] and experimental data, implemented in Verilog-A, and tested with SPICE circuit simulator.

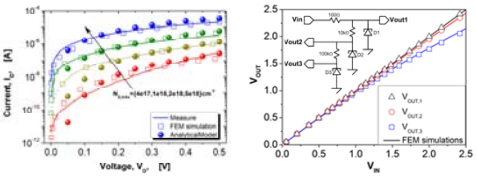


Fig. 5: Left: comparison of the current predicted by the analytical model with numerical simulation and measurements of the Si-InAs diodes fabricated by IBM [5]. Right: Comparison between a SPICE circuit simulation based on our Verilog-A analytical model, and a mixed-mode TCAD FEM simulation.

The Band-to-Band tunneling analytical model developed for the p-n junction has also been applied for the calculation of the carrier flux injected from the source into the channel of Tunnel-FET devices. The current predicted by our model shows a good agreement with numerical simulations.

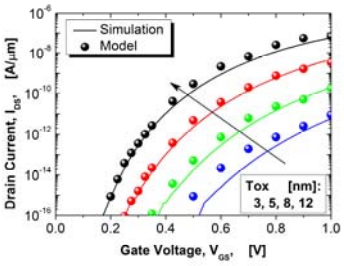


Fig. 6: Comparison of the TFET analytical model we have developed with the transfer characteristic obtained from a TCAD FEM simulation.

CONCLUSIONS A proper modeling of TFET devices requires full quantum approaches which are very accurate but at the same time also demanding from a computational point of view. The benchmarking of FEM simulations with advanced quantum transport models and against experimental data, show that TCAD tool is a mature technique allowing for device optimization and helping the development of analytical and compact model necessary for the success of Tunnel-FET technology.


ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich
*Integrated Systems Laboratory*

IBM
IBM Research - Zurich
CH-8803 Rüschlikon, Switzerland

EPFL
ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE
NanoLab