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Multi-Channel Sensor Front-End for Biomedical Applications

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Abstract – Sensing biomedical signals, i.e., electrical potentials caused by neural activity, is a necessity in clinical diagnostics, e.g., for heart disease detection. Miniaturization is a prerequisite for portable devices which can be used for ambulant long-term monitoring. Besides the diagnostic purpose, small-sized and low-power devices for biomedical data acquisition are interesting for brain-machine interfaces, such as prosthesis control.

A multi-channel sensor front-end ASIC for electroencephalography (EEG), electromyography (EMG) and electrocardiography (ECG) data acquisition is presented.

Typical biomedical signals, as they are recorded for ECG, EMG, and EEG are a superposition of a low-amplitude small signal and an up to three orders of magnitude higher offset (Fig. 1). Signal processing is rendered more difficult by a slight drift of this offset over time due to variations of the skin-to-electrode resistance. The frequency band of interest for most biomedical applications is between 0.5 and 3 kHz and therefore sensitive to flicker-noise. Signal amplitude and bandwidth are dependent on the application: Typical ECG (EMG/ EEG) signals have an amplitude of up to 5 mV (1 mV/ 100 µV) and frequencies between 0.5 and 100 Hz (3 kHz/ 100 Hz).

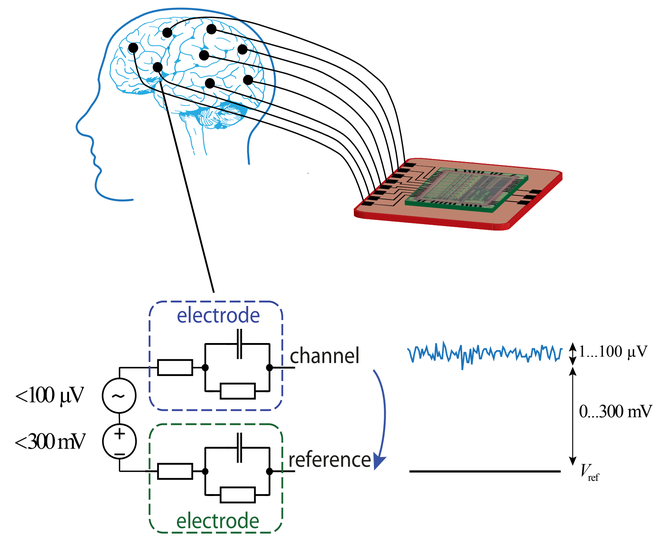

Fig. 1: Surface EEG signals typically have a small signal (> 0.5 Hz) amplitude of 100 μV_{pp} while they are superimposed to a time variant offset of up to 300 mV.

Circuit

An overview on the implemented circuit is shown in Fig. 3. The integrated circuit (IC) allows to digitize eight channels simultaneously. While a separate analog front-end was implemented for each channel. The analog-to-digital converter (ADC) is shared among the channels. Prior to amplification, the signal offset is compensated with a current-steering digital-to-analog (DAC) converter to prevent the instrumentation amplifier (IA) from saturation. This DAC is regulated by off-chip digital circuitry, since the offset is not constant . A second DAC compensates the IA offset.

Chopping [1,2] is used to suppress the flicker-noise added by the IA (Fig. 2, 6). To avoid aliasing, the modulated offset and flicker-noise is damped with an active low-pass filter (LPF) with a corner frequency of 3.2 kHz which limits the (analog) bandwidth. The gain of the front-end is adjustable between 128x and 2048x to address different signal amplitudes.

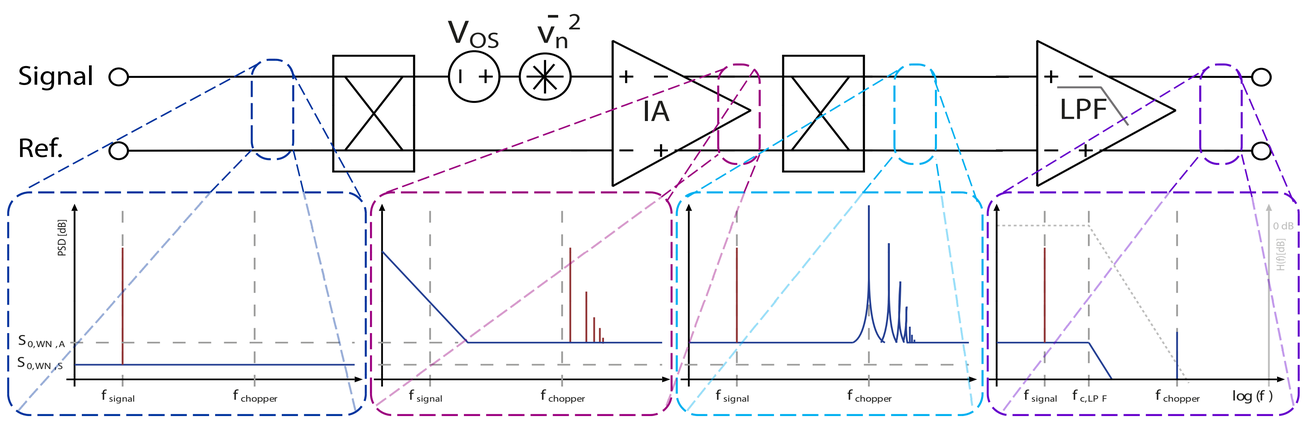

Fig. 2: The principal idea of chopping is to modulate the low-frequency flicker-noise added by the instrumentation amplifier (IA) to an out-of-band frequency: (f.l.t.r.) A first chopper modulates the input signal to $f_{chopper}$ and its odd harmonics. This signal is fed into the instrumentation amplifier, which typically adds offset, flicker and thermal noise to the amplified signal. In this figure an amplification by 1 (0 dB) is chosen for simplicity. A second chopper modulates the amplifier's output. While the amplified input signal is demodulated, the added noise is modulated to the chopping frequency and its odd harmonics. Finally the signal is low-pass filtered.

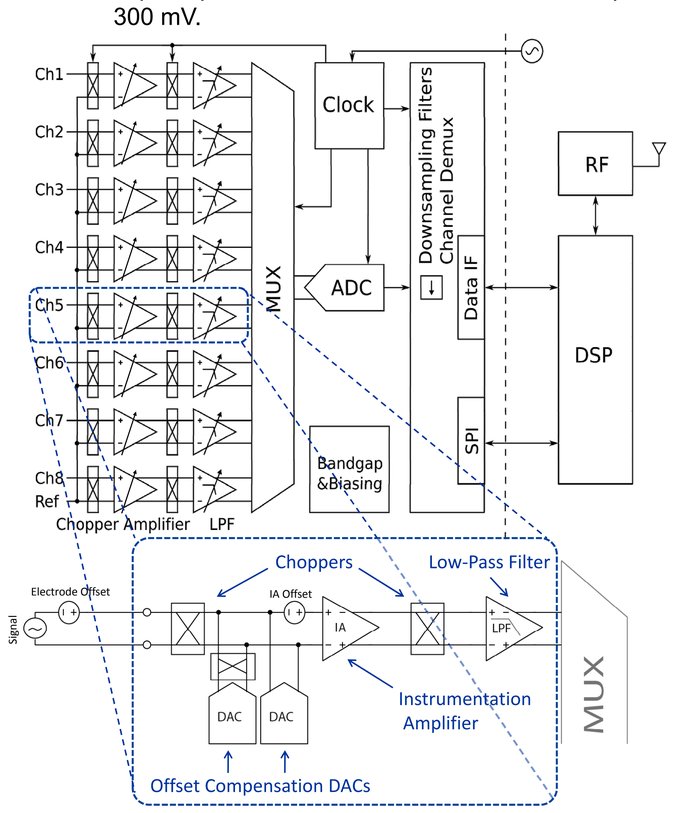

Fig. 3: Diagram of the implemented circuit with a detailed illustration of one channel's analog front-end: Chopping is used to suppress flicker noise while compensation DACs are necessary to remove the rather large (near) DC part of the signal prior to amplification.

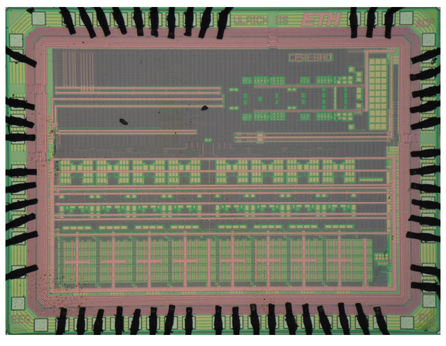

Fig. 4: Photomicrograph of the multi-channel sensor front-end ASIC named "Cerebro".

Table 1: Performance Summary

Max. SFDR	66 dB
Max. Input Swing	9 mV
Analog Bandwidth	3.2 kHz
System Bandwidth	0.5/ 1/ 2/ 4 kHz
IR-Noise (mean over freq.)	~ 82 nV/√Hz
Supply Voltages	1.2 V / 3.3 V
Technology	130 nm
Typical Values for EEG	
Signal Amplitude	100 µV
SNDR (1…100 Hz)	32 dB
SFDR (freq. independent)	49 dB
RMS Noise (1…100 Hz)	0.81 µV

Measurement Results

The circuit has been fabricated in a 130 nm CMOS technology (Fig. 4). The analog front-end is in general limited due to noise, not due to distortion. Therefore, the spurious-free dynamic range (SFDR) is significantly higher than the signal-to-noise-ratio (SNR). Thanks to chopping, the noise-floor is nearly constant over frequency (Fig. 6) and was measured to be roughly 82 nV/√Hz.

A performance test measurement for the typical EEG conditions for amplitude and signal band is shown in Fig. 5. For a sine-wave of 100 μV_{pp} magnitude a SFDR of 49 dB is measured while the signal-to-noise-and-distortion-ratio (SNDR) over the 1 Hz to 100 Hz frequency band, which is typically used for EEG, is 32 dB.

The efficacy of the flicker-noise suppression by chopping [1,2] is demonstrated in Fig. 6: It compares a measurement of the noise floor with chopping enabled to a case for which the choppers are disabled. The noise is significantly reduced in the frequency band of interest.

Table 1 gives a performance summary, a in-vivo test showing a ECG measurement recorded with "Cerebro" is depicted in Fig. 7.

[1] C.C. Enz and G.C. Temes, "Circuit Techniques for Reducing the Effects of Op-AmpImperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization", Proceedings of the IEEE, Nov. 1996.

[2] Q. Huang and C. Menolfi, "A 200 nV Offset 6.5 nV/√Hz Noise PSD 5.6 kHz Chopper Instrumentation Amplifier in 1 mm Digital CMOS", IEEE ISSCC, 2001.

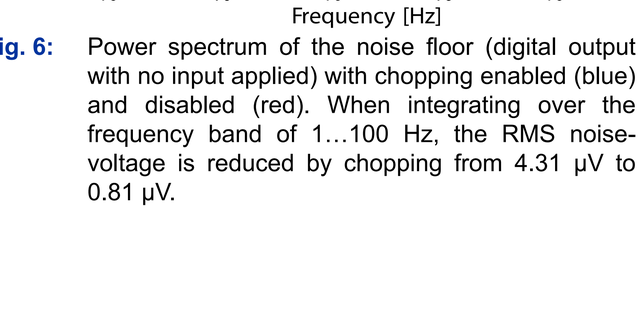

Fig. 5: Power spectrum of the digital output for an applied test-signal of 100 μV_{pp} at 11 Hz. The noise was integrated for a typical EEG band of 1…100 Hz.

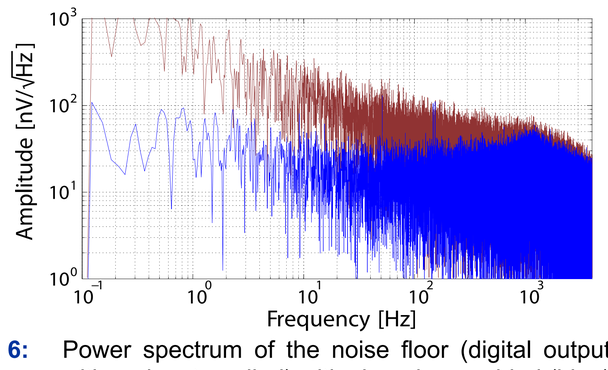

Fig. 6: Power spectrum of the noise floor (digital output with no input applied) with chopping enabled (blue) and disabled (red). When integrating over the frequency band of 1…100 Hz, the RMS noise-voltage is reduced by chopping from 4.31 µV to 0.81 µV.

Fig.7: In-vivo ECG measurement using one channel of "Cerebro".