

Wirelessly Powered Sensor Node for Bio-Medical Applications

Xiao LIU and Catherine DEHOLLAIN

École polytechnique fédérale de Lausanne (EPFL) -RFIC, 1015 Lausanne



The Main Objective:

To develop wirelessly powered integrated circuit in nano-scaled CMOS technologies which acquires data from various types of sensors. The circuit should also wirelessly communicate with the base station.

Sensor Interface:

For medical implants, the sensor interface converts the various physiological signals into digital codes for further processing. For example, the bandwidth and magnitude of bio-electric signals are shown on the right, which are in the order of uV to mV and the frequencies span from DC to a few kHz. The sensor interfaces are composed by the pre-filter/amplifier, analog-digital convertor (ADC) and calibration circuits if necessary.



Applications:

- Sensors monitoring vital signals in humans such as ECG, blood pressure and body temperature.
- Implanted sensors in animals in order to study their physiology or behavior.
- Sensor monitoring environment such as pollution and temperature.
- Security applications like cameras, microphone and gas sensors.

For a first demonstrator we will implement a system which measures the body temperature of mouse in order to study its metabolism to prevent obesity.

Example Applications:

- Implanted circuit to monitor blood pressure of mouse [P. Cong et al., "A Wireless and Batteryless 10-Bit Implantable Blood Pressure Sensing Microsystem With Adaptive RF Powering for Real-Time Laboratory Mice Monitoring," IEEE Journal of Solid State Circuits, Dec. 2009].



Considering for different medical applications, the sensor node must be compatible with a variety of sensors, each of which corresponds to particular specifications. It is necessary to provide multiple frond-end amplifiers and filters, or to implement programmable circuits which provides various gain and pass band. One example is shown in the system block diagram, where the sensor interface circuits consists of multiple signal paths, where a particular path is activated according to application.





- Batteryless patch sensor for ECG monitoring [J. Yoo et al., "A 5.2 mW Self-Configured Wearable Body Sensor Network Controller and a 12 uW Wirelessly Powered Sensor for a Continuous Health Monitoring System," IEEE Journal of Solid State Circuits, Jan. 2010].

Demonstrator:

Using commercial components, a remotely powered sensor node and its base station is implemented. With this setup, it's possible to illustrate the principle of wireless power transmission and communication.







375 Hz

12 Kbps

8 bits

180 uW

Data Out

Currently, the project is focusing on a temperature monitoring application for mouse. A micro thermistor is used for temperature sensing, which provides a voltage responds of 3.8mV/0.05°C at 1.8V voltage excitation. In order to measure the offset of the interface circuits, a four-wire measurement is used. The signal is chopped to 10KHz frequency, and processed by the front-end circuits, which amplify the signal to meet the dynamic range of the ADC and provides low pass filtering. Afterwards, the signal is converted by a 8-bits, 1Ms/s SAR ADC with a over-sampling rate of 50. The schematics for the interface circuits are shown above. The specifications of thermistor are shown in the Table.



Parameters	Value
Resistance@+25°C (kΩ)	100
Response time in liquids (ms)	200
Dissipation constant in still air (mW/°C)	0.3
Resistive Response (Ω/0.05°C)	200

BethaTerm Sensor: www.betatherm.com

Analog-Digital Convertor:

One ADC chip has been fabricated in 0.18um CMOS technology, which is a 8-bit SAR ADC with 8 parallel outputs.





The sensor interface of the demonstrator is composed by four parts, which includes a front-end amplifier, a ADC, a voltage regulator and a clock divider. The front-end circuits extracts the sensor output as a voltage difference between the sensing bridge and the reference bridge. A amplifier amplifies the signal to meet the dynamic range of ADC. The regulator provides a stable 1.8 V voltage to drive the ADC chip, and the clock divider generates the chip select and internal clock signals for the ADC. The digital output codes of the ADC is serial, and would be sent back to the base station through transmitter. The data rate of the transmission is 12 Kbps, which corresponds to a maximum of 380 Hz sampling rate. Under this configuration, the interface circuits consumes approximately 180 uW.

The chip is tested with a 5KHz sinus wave at its input. The clock frequency is at 2MHz, which corresponds to a 200KHz of sampling rate. According to the FFT of the output digital codes, the signal processes a total SNDR of 43dB, which leads to a 6.7 bits ENOB. Under this configuration, the total power consumption of the core circuit is 20 uW. In order to further reduce the power consumption, it's possible to reduce the clock frequency.

Measurement Results	
Resolution	8 bit
Sampling Rate	200 KHz
ENOB	6.7 bits
Power Consumption	20 uW