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Complementary BAW oscillators for Ultra-Low Power Consumption and Low Phase Noise

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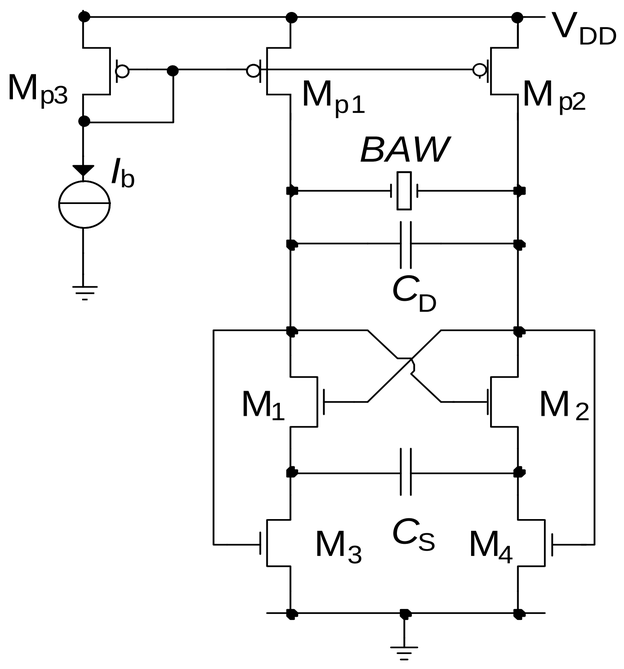
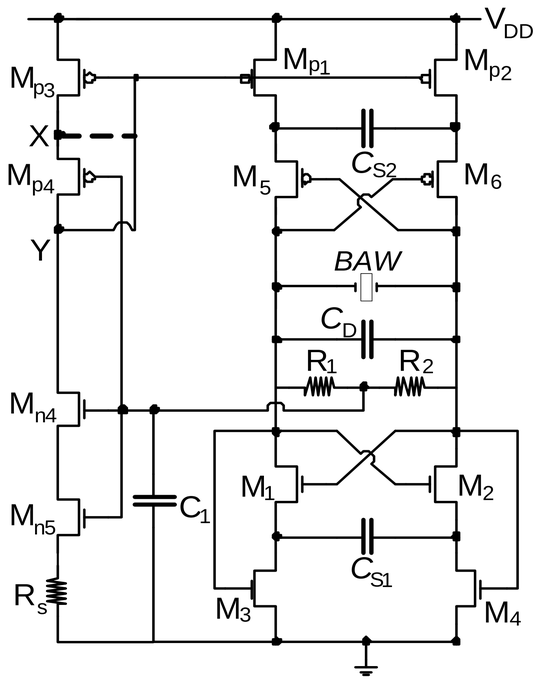
A complementary cross coupled BAW parallel resonance oscillator offering ultra-low power consumption and a good phase noise performance is presented. The power consumption in this structure is 50% less than the classical NMOS based structure without any penalty in the phase noise performance. Rather, this structure serves to reduce the noise contribution of the biasing transistors at the output leading to a marginal improvement in thermal noise performance as compared to the NMOS based structure. Furthermore, the flicker noise upconversion of this complementary structure can be minimized by proper design.

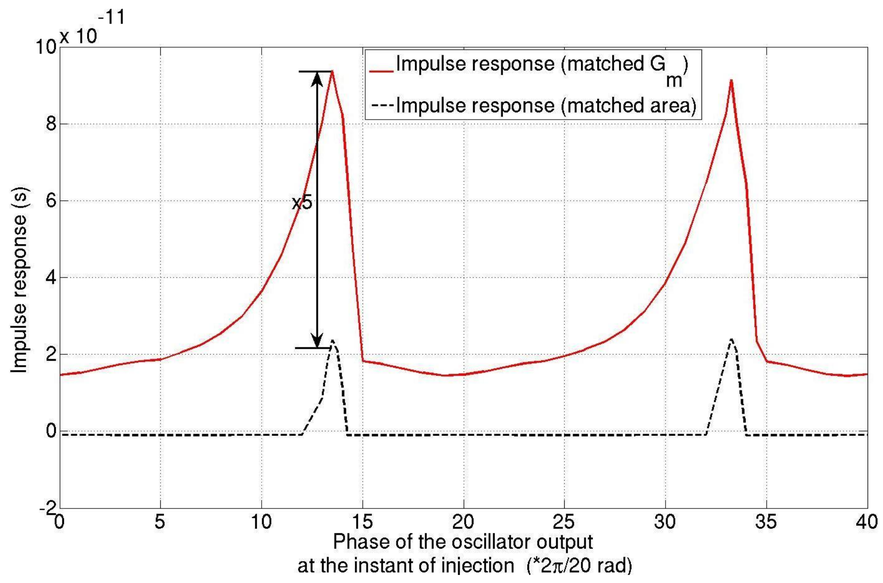
Complementary BAW oscillators



NMOS CROSS-COUPLED (C-C) BAW OSCILLATOR



COMPLEMENTARY BAW OSCILLATOR



ISF COMPARISON –
Gm MATCHED VS AREA MATCHED TOPOLOGIES

POWER CONSUMPTION

- The power consumption in weak inversion
$$P = \kappa \cdot V_{DD} \cdot 2G_{mcrit} \cdot nU_T$$
- Complementary structure: $G_{mcrit} = R_m C_L^2 \omega_0^2$
- NMOS c-c structure: $G_{mcrit} = 2R_m C_L^2 \omega_0^2$
- So, ideally : $P_{complementary} = \frac{1}{2} P_{NMOS}$
for same output signal amplitude.

THERMAL NOISE

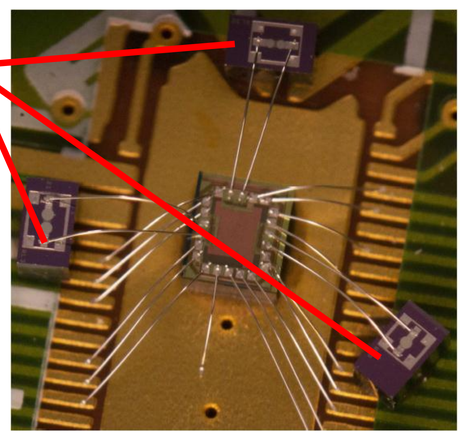
- Total Noise of the cross coupled (c-c) pair - approx. same for same amplitude for NMOS c-c and complementary structures.
- Noise of the CMFB transistors - negligible in both cases.
- Noise from the current mirror - negligible for the complementary structure.
- The total noise at the output is lower for the complementary structure due to an increase in load capacitance
i.e. $Phase\ noise\ \alpha\ \frac{1}{C_{LOAD}^2}$

FLICKER NOISE

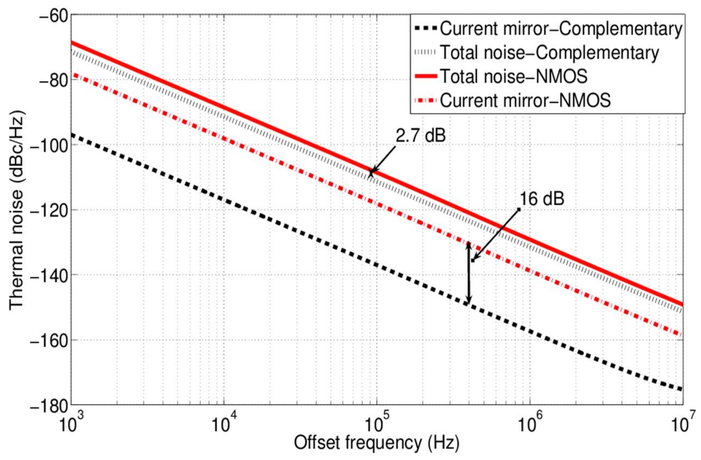
- Complementary structure- Biasing transistor not connected to output unlike NMOS c-c structure.
- Sizes of these transistors can be increased to reduce their flicker noise without increasing power.
- Complementary structure : Optimization of flicker noise – Matching between the NMOS and PMOS c-c pair (Match in area / Match in G_m).
- Impulse sensitivity Function (ISF) simulation shows that c-c pair area-matched topology has the best flicker noise performance.

Results & Conclusions

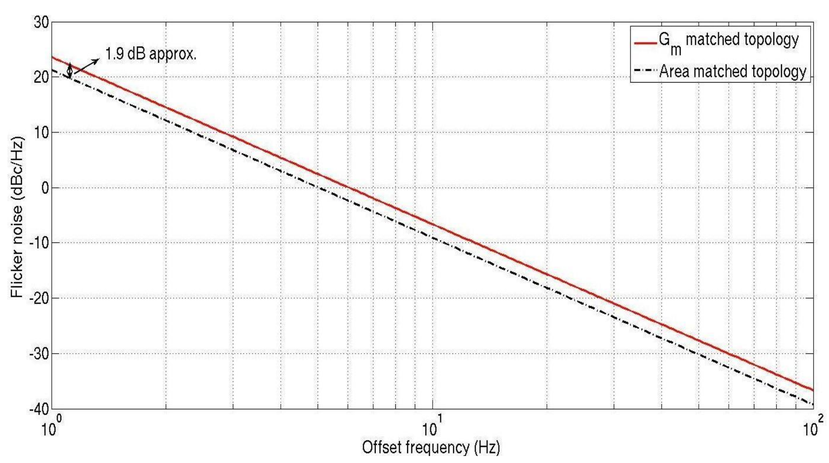
BAW resonator



MICROPHOTOGRAPH OF THE CHIP



THERMAL NOISE COMPARISON –
COMPLEMENTARY VS NMOS CROSS-COUPLED



FLICKER NOISE COMPARISON –
Gm MATCHED VS AREA MATCHED TOPOLOGIES

	Complementary structure	NMOS based structure
Frequency	2.537 GHz	2.545 GHz
Power Consumption	667.5 μW	1177.5 μW
Flicker Noise @ 1 Hz offset	21.18 dBc/Hz	26.278 dBc/Hz
FOM @ 1 Hz offset	105.585 dB	96.07 dB
Thermal Noise @ 100 kHz offset	-119.02 dBc/Hz	-115.87 dBc/Hz
FOM @ 100 kHz offset	194.03 dB	188.425 dB

COMPLEMENTARY STRUCTURE VS NMOS BASED STRUCTURE – PERFORMANCE

Conclusions

A complementary structure based BAW resonator oscillator at 2.53 GHz which consumes around 670µW power for achieving an amplitude of 300mV has been demonstrated in this work. A comparison with the NMOS based structure reveals that complementary structure has half the power consumption due to increased negative resistance at the same bias current. Further, there is a marginal improvement in the case of the latter due to better filtering of noise of biasing transistors for the same amplitude. This results in a gain of around 5dB in *1/(Power*Phase Noise)* Figure of Merit. Also, by using an area matched topology for the NMOS and the PMOS cross-coupled pairs in the complementary structure, a flicker noise performance better than that of the NMOS based structure can be achieved.

R.Thirunarayanan, A. Heragu, D. Ruffieux, and C. Enz, NewCAS, June 2011 (Best Student Paper Award)