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A Reconfigurable Transceiver for Power-Efficient Long-Distance Transmission of Variable-Rate Multi-Source Sensor Data

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***Abstract** – Sensor networks deal intrinsically with low-bandwidth signals, and therefore low data-rates for their transmission. However, multiple channel data are often aggregated together locally leading to higher data-rates requirements for their long distance transmission. Such data-rates can either be accommodated by a low-speed communication standard (GSM/EDGE) with high duty-cycle or by high-speed standards (WCDMA/LTE) with low duty-cycle, which is generally more power efficient. A reconfigurable direct-conversion transceiver designed for several standards, from GSM to LTE, is capable of supporting a wide variety of sensor networks requirements in a power efficient way.*

1. Power-Efficient Transmission

- ❑ Low-duty cycle transmission proves to be power efficient
- ❑ Memory needed to store acquired sensors data
- ❑ An optimum is found as a trade-off between data-rate and memory cut

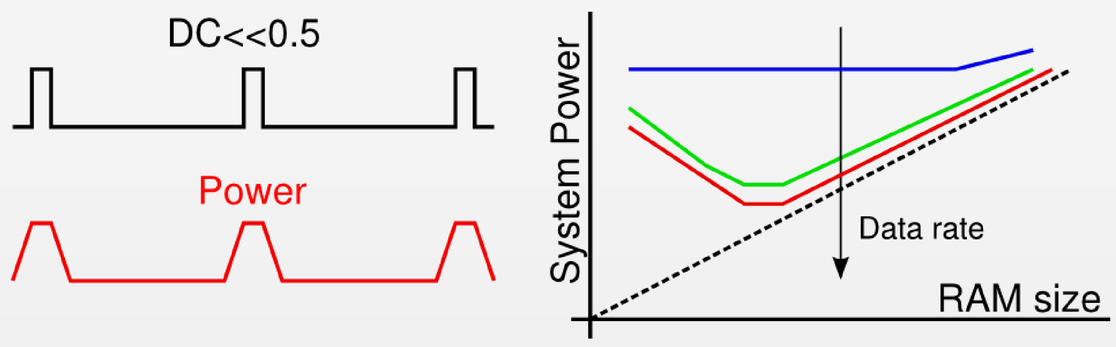


Fig. 1: Conceptual low DC transmission (left) and power trend vs. data-rate and memory cut (right).

2. Direct Conversion Transceiver

- ❑ Programmable signal bandwidths up to 10MHz
- ❑ SAW-less implementation thanks to high linearity
- ❑ Receiver filter gain scalable vs. ADC dynamic range

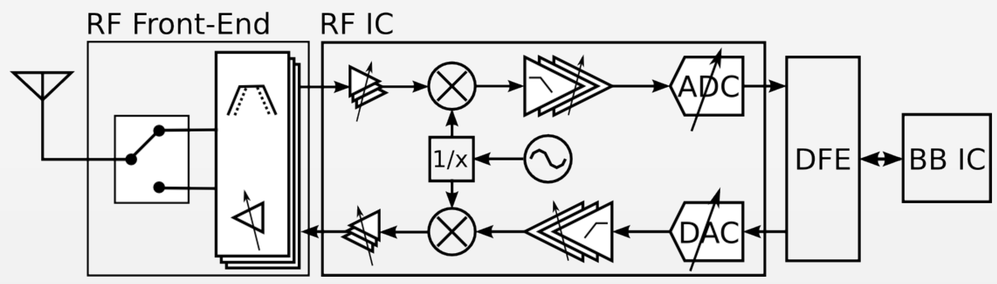


Fig. 2: Architecture of the reconfigurable transceiver.

3. Receiver A/D Conversion

- ❑ Multi-bit DT Sigma-Delta modulator in 130nm CMOS [1]
- ❑ Scalable signal bandwidths between 100kHz and 25MHz
- ❑ Programmable OSR from 130 (GSM/EDGE) to 10 (LTE-Advanced)

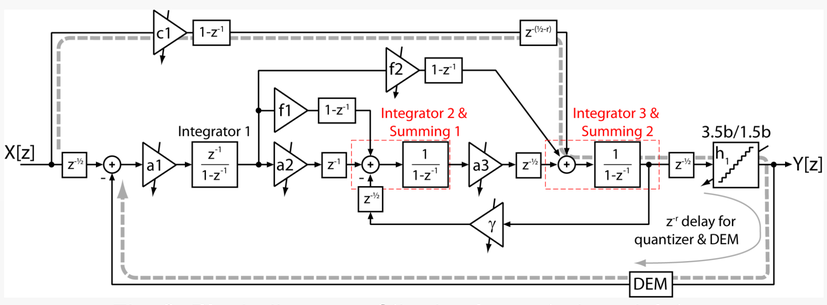


Fig. 3: Block diagram of the implemented modulator.

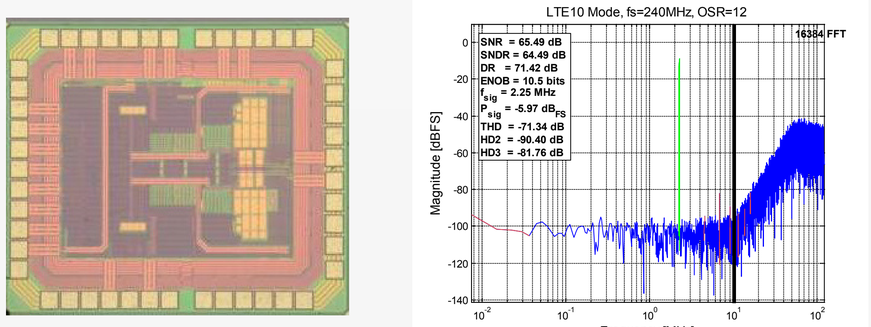


Fig. 4: Chip micrograph (left) and measured output spectrum for a 2.25MHz input signal (right).

4. Transmitter D/A Conversion

- ❑ 10 bits current-steering DAC in 130nm CMOS [2]
- ❑ Programmable bandwidths of 1.35MHz, 4.5MHz and 9MHz
- ❑ Scalable power consumption between 1.2mW and 3.96mW

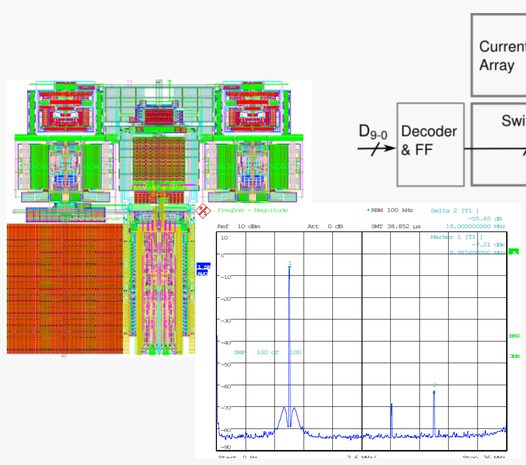


Fig. 5: Chip layout (left) and measured output spectrum for a 9MHz input signal (right).

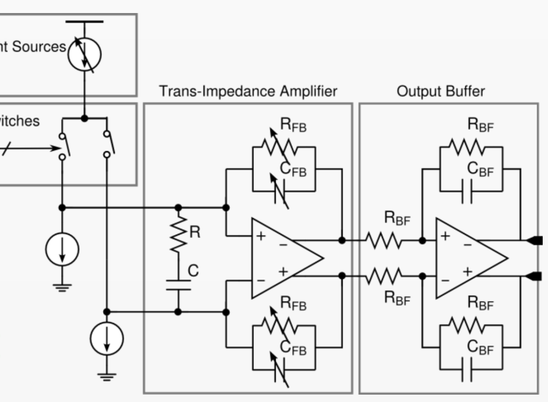


Fig. 6: Topology of the implemented current-steering DAC. Programmability is obtained over the RC coefficients.

5. Frequency Synthesizer

- ❑ GSM/WCDMA/LTE fractional-N synthesizer in 130nm CMOS [3]
- ❑ 25Hz frequency resolution
- ❑ Programmable loop bandwidth from 30kHz to 140kHz
- ❑ Settling time lower than 65us to 1ppm
- ❑ Power consumption between 62mW (GSM) and 32mW (LTE)

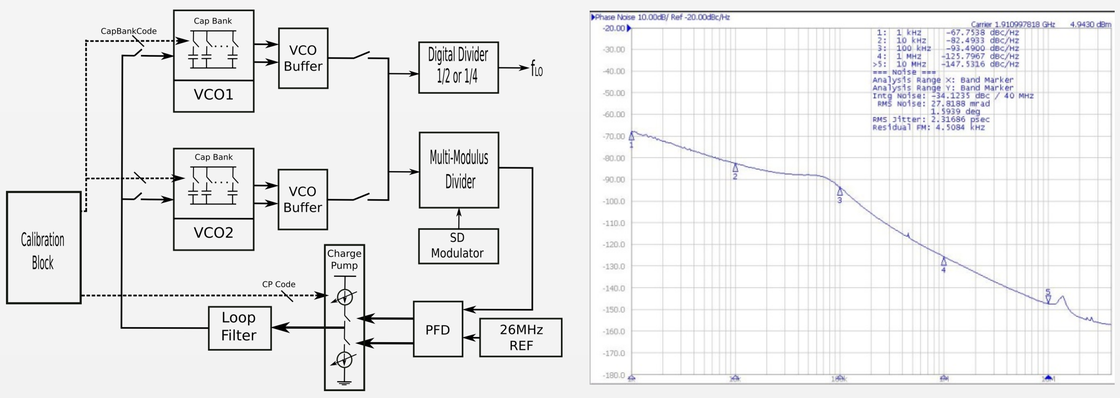
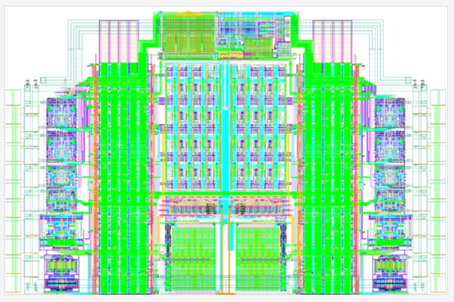


Fig. 7: Synthesizer topology (left) and measured phase noise for the GSM mode (right).

6. Base-Band Filters

- ❑ 4th order Chebyshev Tx filter in 130nm CMOS
- ❑ 6th order Chebyshev Rx filter in 130nm CMOS
- ❑ Programmable gain and tunable cut-off frequencies Rx (170kHz to 9MHz) Tx (2.5MHz to 12.5MHz)



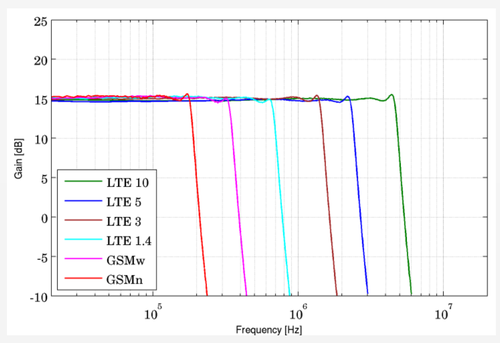


Fig. 8: Tx chip layout (left) and measured Rx transfer function for different modes (right).

References:

[1] T. Christen, Q. Huang, “A 0.13um CMOS 0.1-20MHz BW 86-70dB DR Multi-Mode DT ΔΣ ADC for IMT-Advanced”, Proc. ESSCIRC 2010.

[2] N. Ghittori et al., “1.2-V Low-Power Multi-Mode DAC+Filter Blocks for Reconfigurable (WLAN/UMTS, WLAN/Bluetooth) Transmitters”, IEEE JSSC, vol.41, no.9, pp.1970-1982, Sep. 2006.

[3] E. Hegazi, H. Sjoland, A. Abidi, “A filtering technique to lower LC oscillator Phase Noise”, IEEE JSSC, vol.36, no.12, pp.1921-1930, Dec. 2001.