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CMOSAIC RTD 2009

FNSNF

Intra chip stack fluidic cooling: the CMOSAIC demonstrator

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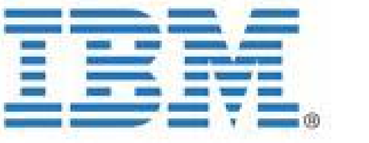
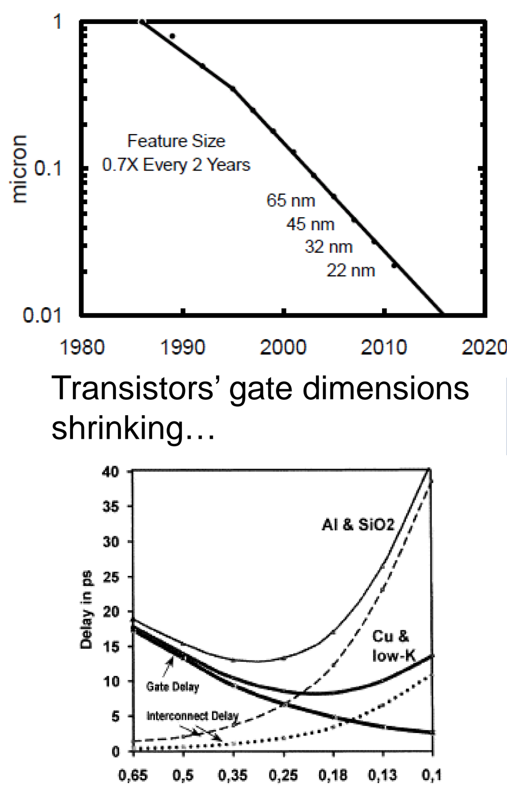


MOTIVATION



Transistors' gate dimensions shrinking…

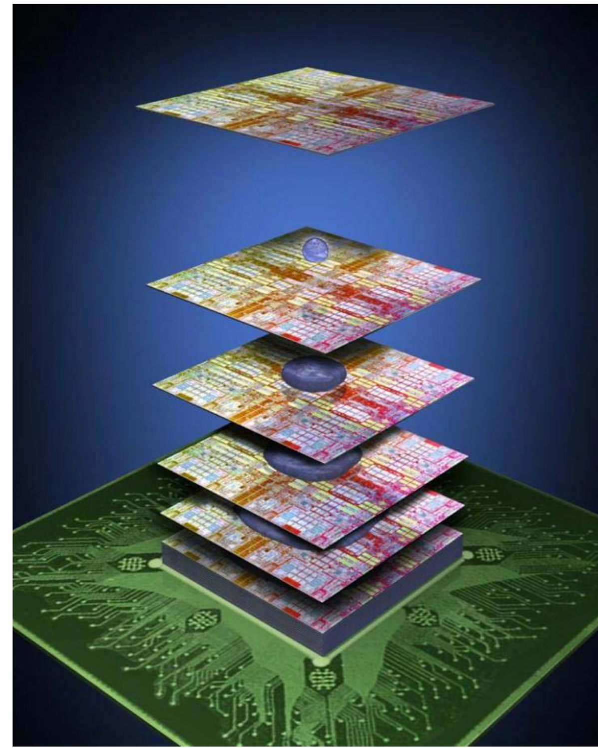
…gate delay vs interconnect (*RC*) delay…

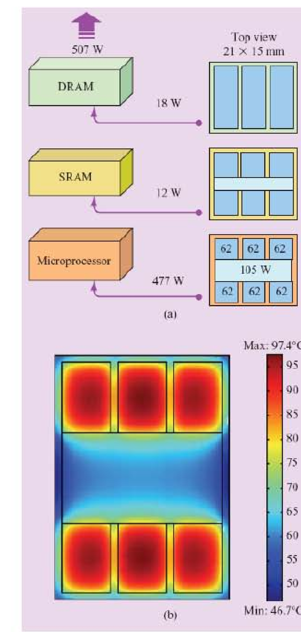
RC delay = $2\rho\varepsilon(4L^2/P^2 + L/T^2)$

- Need to decrease RC delay

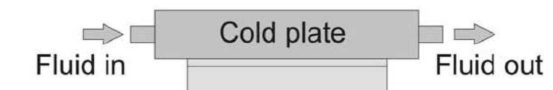
Need to:

- alleviate density (P↗)
- reduce interconnect wire length (L↘)

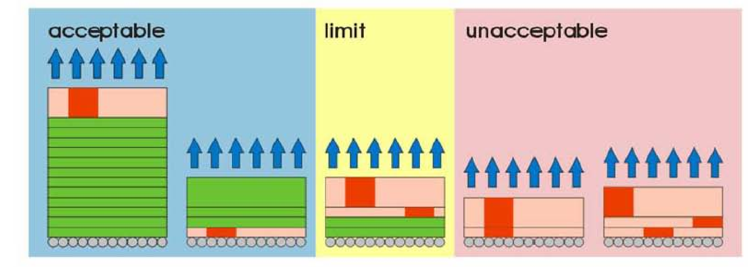




…from 2D interconnects to SOC to 3D interconnects…



Microchannel back-side heat removal



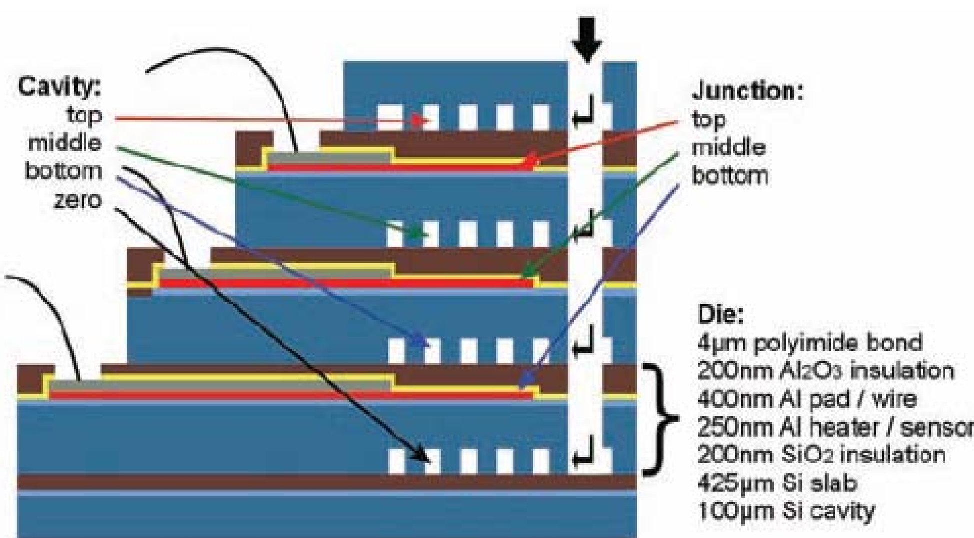
Heat flux and thermal resistance accumulate
Memory to logic heat flux ration: 1:10
Back-side heat removal does not scale with die stacking

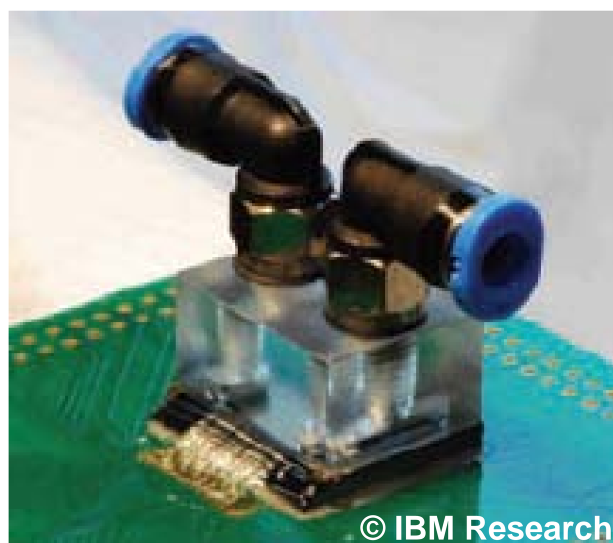
…to the limits of backside cooling…

TO INTERLAYER EMBEDDED COOLING !!

1st generation CMOSAIC interlayer cooling: PYRAMID STACK

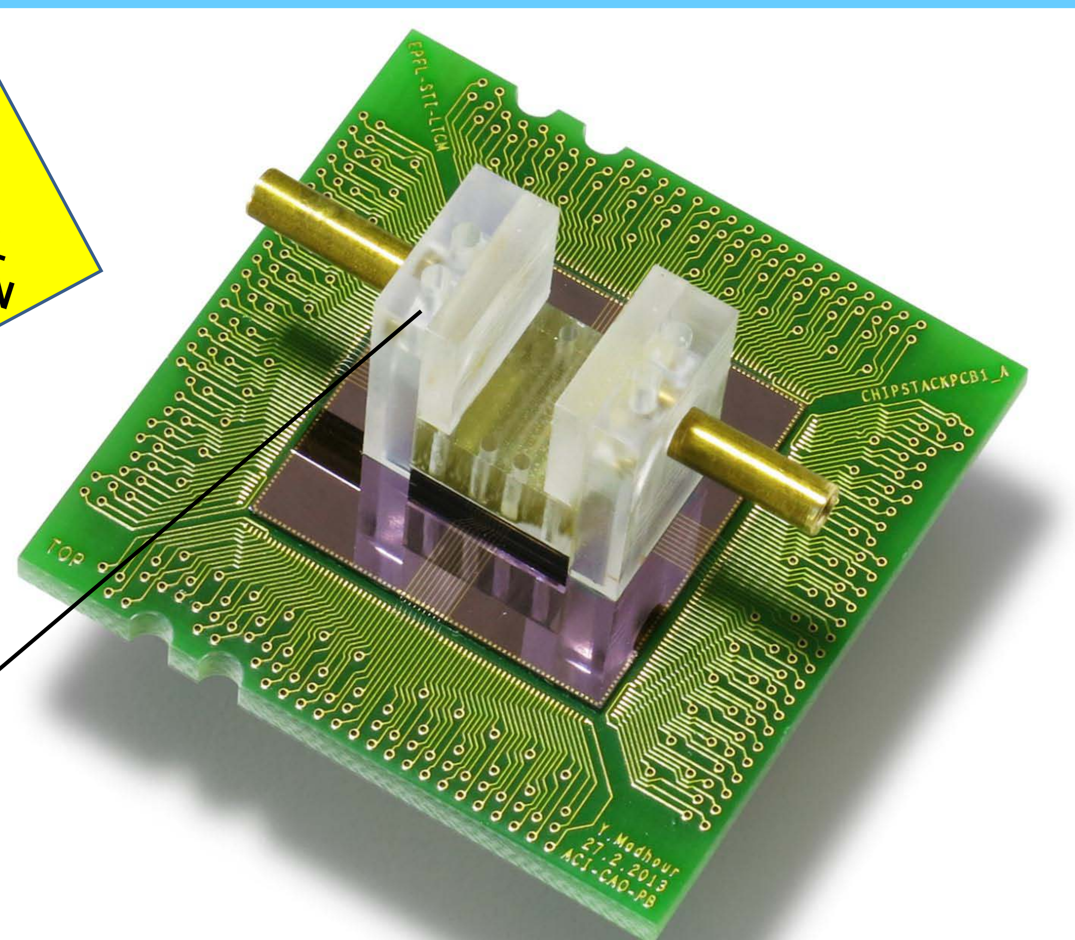
- 5-layer chip stack.
- 4 active levels with layer-embedded cooling structures.
- Heat removal configurations: Silicon microchannels or Si pin fins.
- Stacking: high pressure membrane bonding.
- Polymer die-to-die bonding.
- Individual die power input through wire-bonding.
- Wedge-wedge 25µm Aluminum wires.
- RTDs on every layer for temperature measurements.
- No Through Silicon Vias.





1st generation: PYRAMID STACK

VERTICAL ELECTRICAL INTEGRATION



2nd generation:

CMOSAIC Interlayer Cooling System

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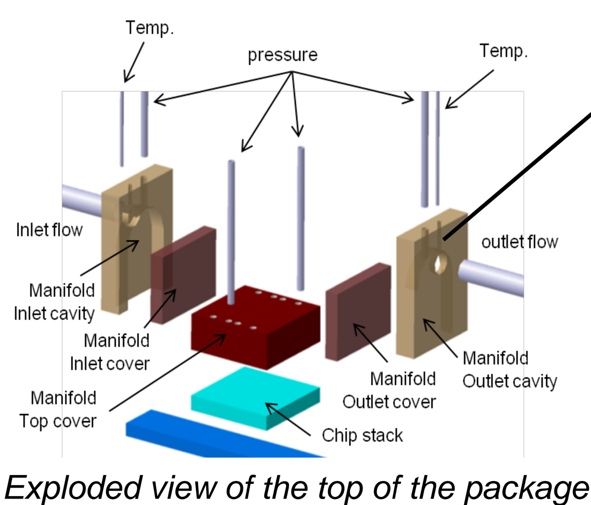
Experimental Heat Transfer and Package Performance Tests

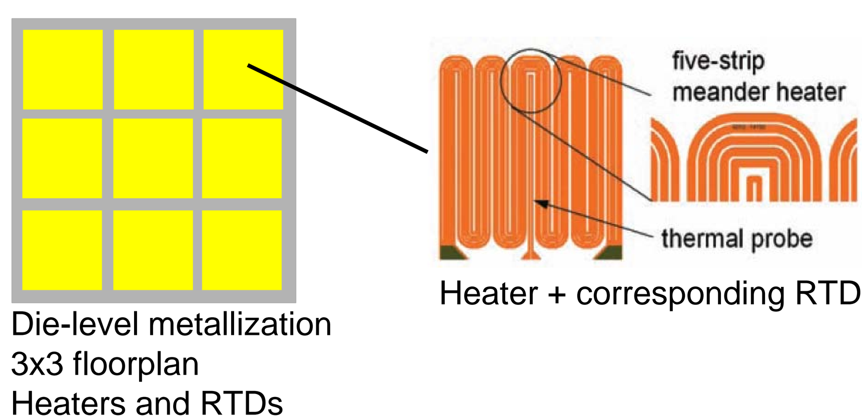


Exploded view of the top of the package

- Manifold for coolant delivery into chip stack.

Possible direct measurements during package operation:

- Accurate local pressures and temperatures of coolant fluid, inside the manifold entrance and exit cavities.
- Accurate coolant pressure drop across entire package.
- Accurate pressure drop across chip-level only, for 2 different levels.
- Additional pressure and temperature (junction and coolant) via Resistance Thermal Detectors (RTDs) deposited at die-level, front side.



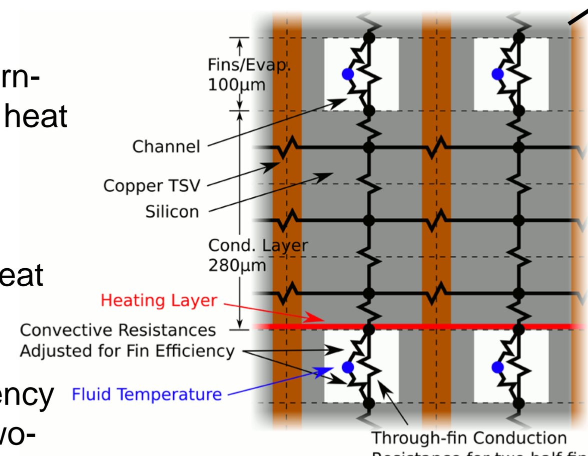
Die-level metallization
3x3 floorplan
Heaters and RTDs

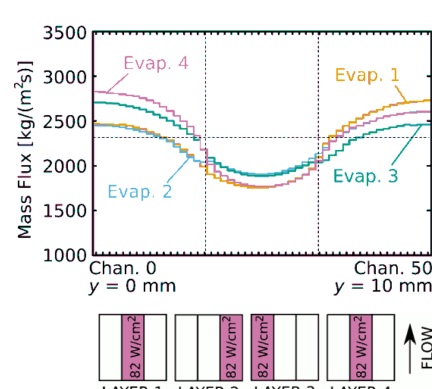
Heater + corresponding RTD

A novel 3D Heat Conduction Model for chip stacks with integrated two-phase cooling

Advantages:

- Accurate, mechanistic, flow-pattern-based methods for microchannel heat transfer and pressure drop.
- Heat spreading: Copper Through Silicon Vias (TSV) included.
- Resolves vertical distribution of heat and thermal resistance between evaporators.
- Careful consideration of fin efficiency and through-conduction for the two-ended fin.
- Allows parametric study for the placement of heat sources within the chip stack.

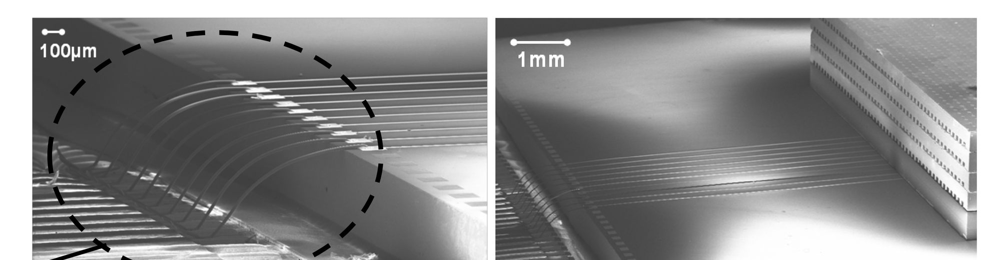




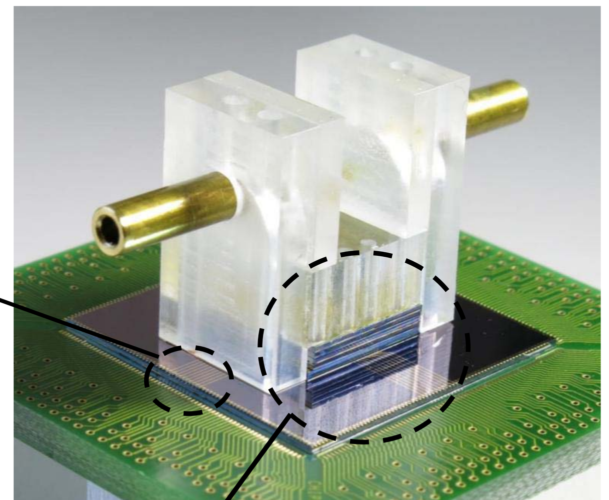
- Same size, shape, and total area of hot spots on each layer.
- Same outlet vapor quality (33%).

Over three fold increased performance due to the consideration of layer interaction effects in hot spot placement

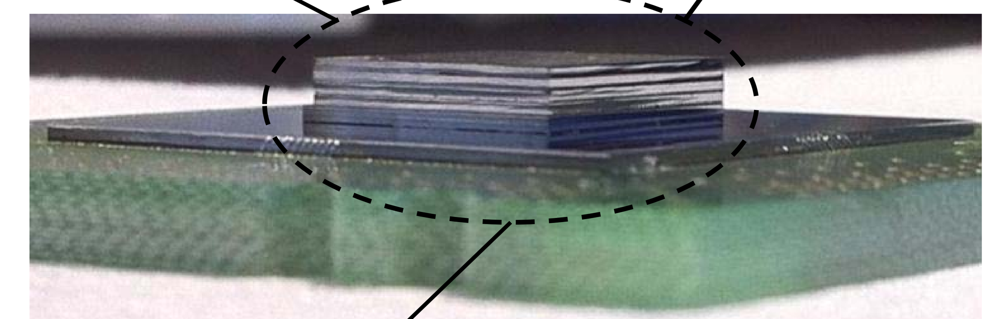
Fabrication & Assembly

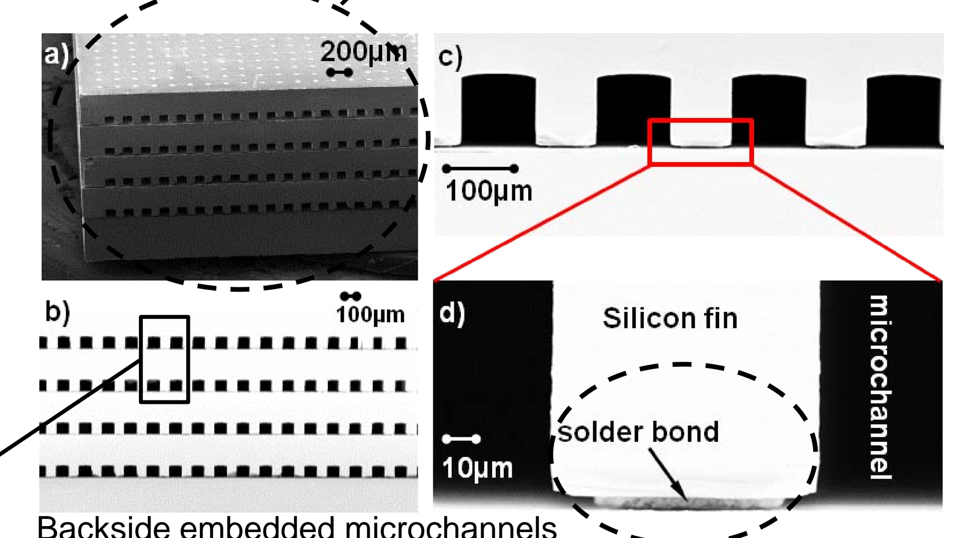


- Silicon interposer chip.
- 22x22mm.
- Interface between PCB and chip stack.
- Wedge-wedge 25µm Aluminum wire-bond.



- 5 layer chip stack.
- chip stack FC bonded to interposer.
- 10x10mm chips.
- 5 electrically active layers.
- 4 layers with embedded cooling structures.
- Stacking via flip-chip (FC) solder bonding.
- Force-controlled reflow process.



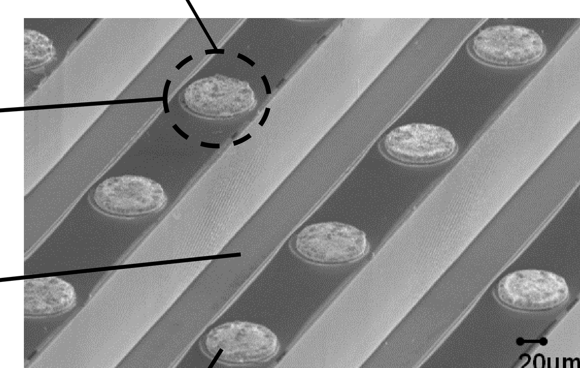


Backside embedded microchannels

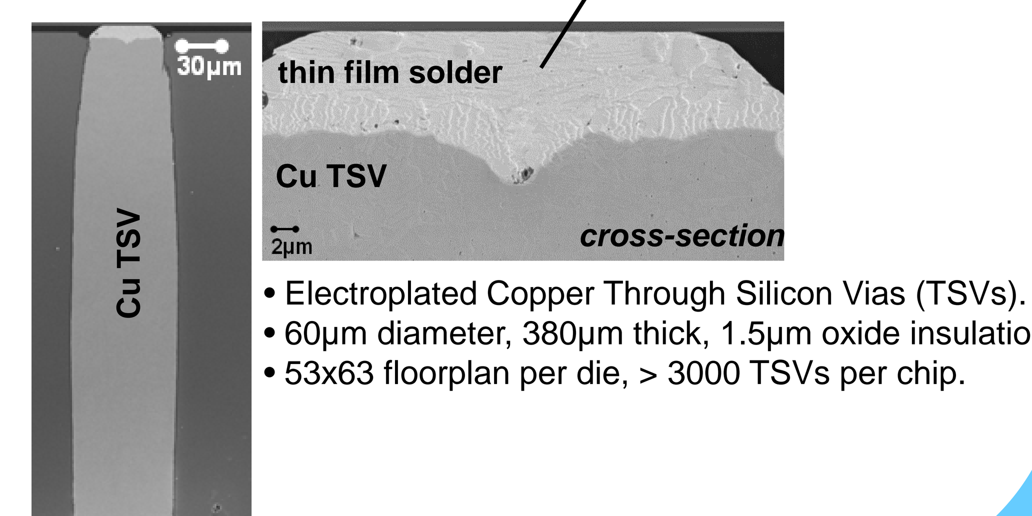
flipped view

- Thin film solder.
- Electroplated on top of TSV surface.
- 58µm diameter.
- 15µm thick after plating.
- 5µm thick after FC bonding.

- DRIE Silicon microchannels.
- 100x100µm .



Single chip bottom view



- Electroplated Copper Through Silicon Vias (TSVs).
- 60µm diameter, 380µm thick, 1.5µm oxide insulation.
- 53x63 floorplan per die, > 3000 TSVs per chip.

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