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Integrated Water Cooled 3D Electronic Chips: Experiments and Modeling

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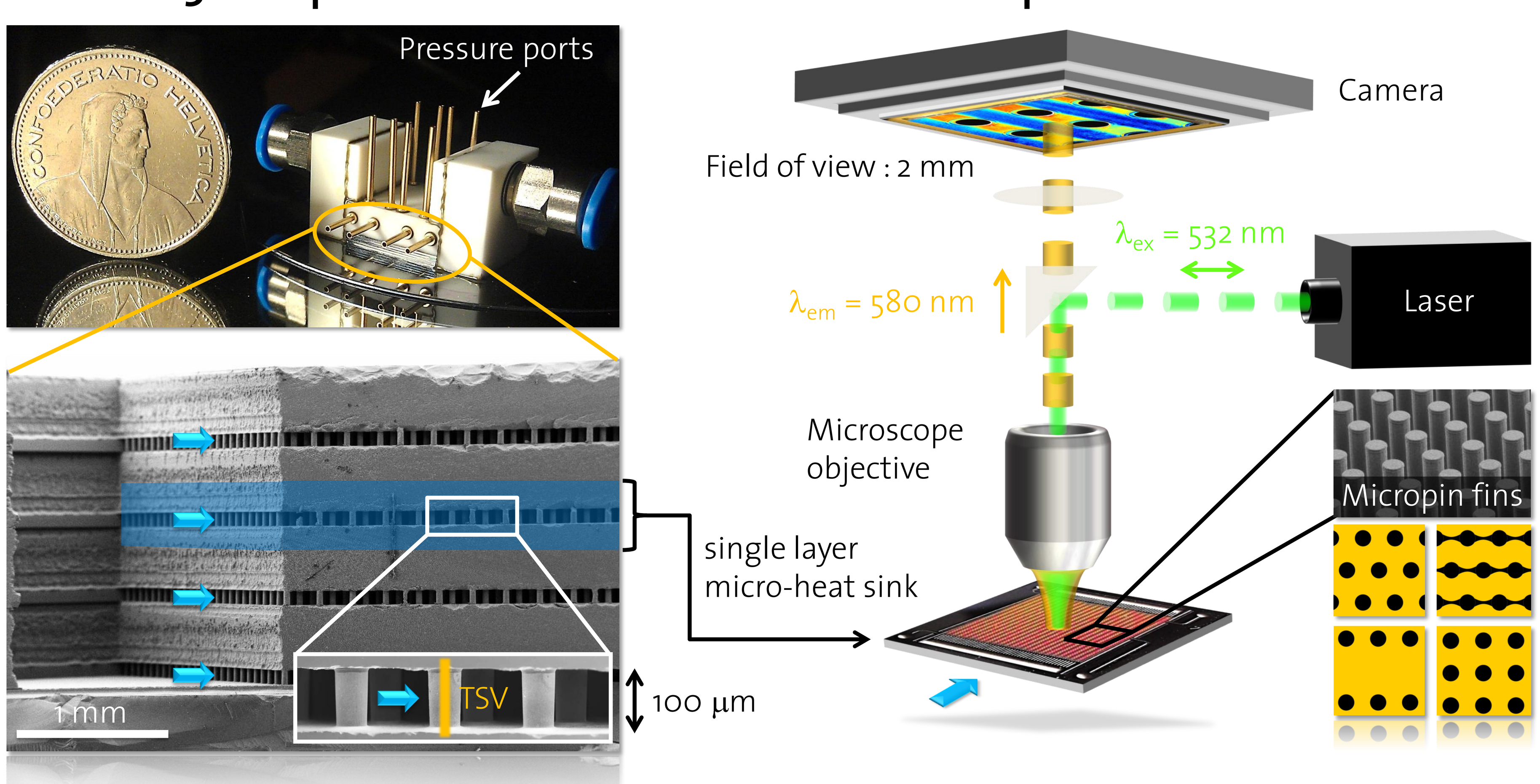
Experiments - We present an integrated water cooling strategy for 3D electronic chip stacks that exploits microscale flow vortices generated by the necessary presence of through-silicon-vias (TSVs), to achieve extraordinary cooling performance. Analysis of microscale flows and instantaneous liquid temperature signatures have opened new frontiers in hydrothermal microscale engineering towards highly efficient micro-heat sinks.

Modeling - In microprocessors, the heat dissipation is not uniformly distributed on the chip surface and different cores (hot-spots) positioning lead to different cooling requirements. The effect of both inhomogeneous hot-spot distribution and pin (TSV) size variation is investigated. Moreover, transition from steady flow to unsteady vortex shedding regime is analyzed on 2D and 3D representative geometries of a chip stack cooling cavity.

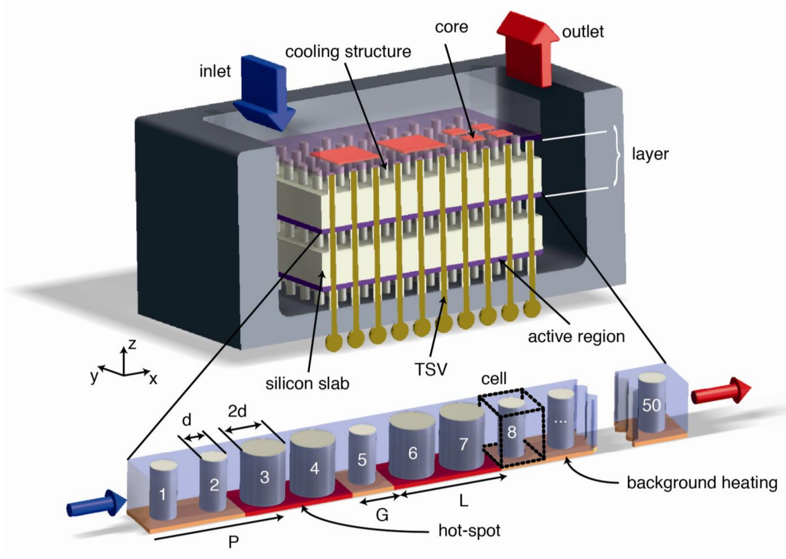
Microscale Thermofluidics

3D chip stack / **Flow and temperature visualization**

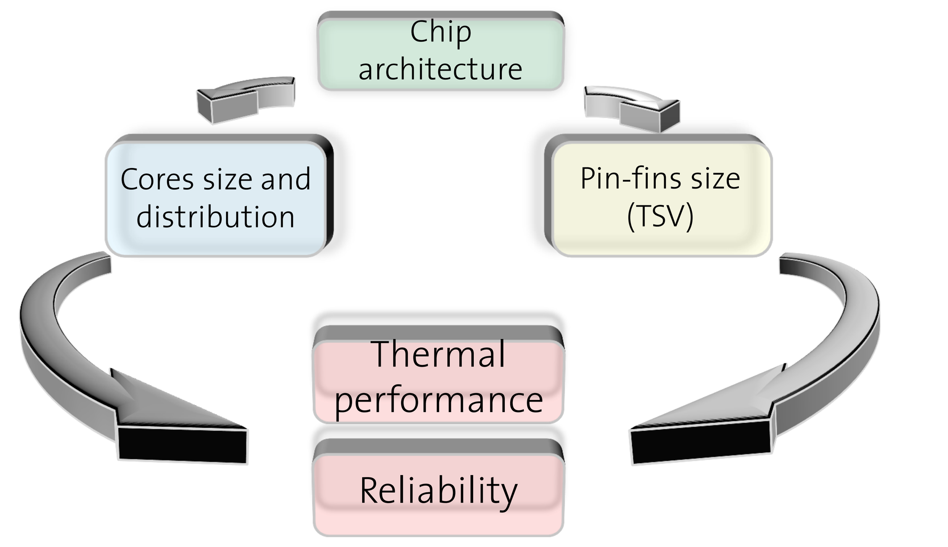


- 3D chip with integrated pressure ports at each microcavity layer
- Confined micropin fins simulate the electrical through-silicon-via (TSV) connections
- Hydrothermal effects were investigated in detail using single micro-heat sink cavities

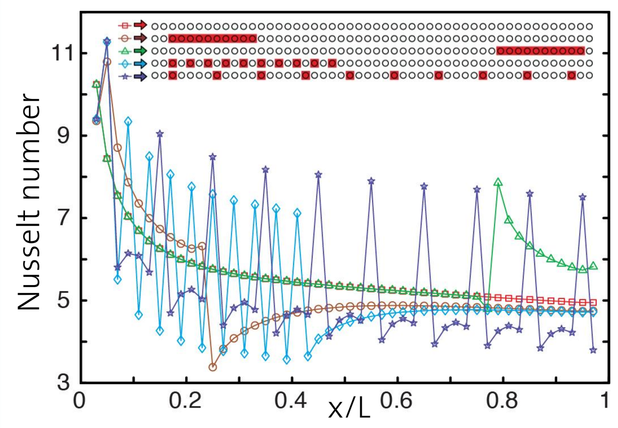
Hot-spots Management



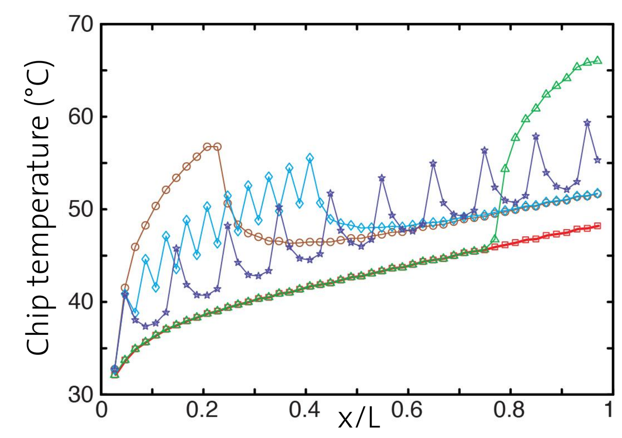
a) Chip stack with representative geometry modeled



b) Hot-spots arrangements and pin diameter variations determine the thermal performances

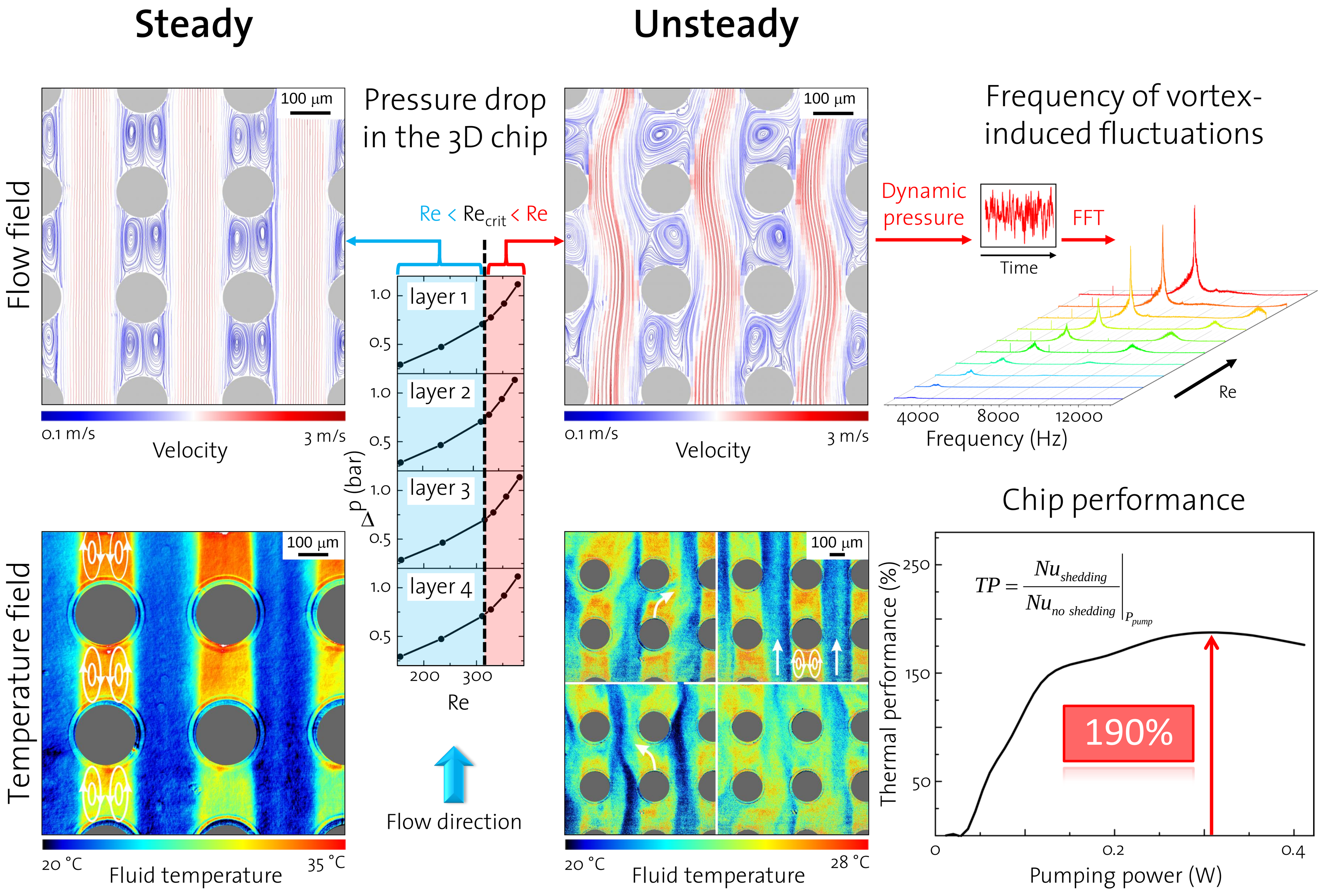


c) Effect of hot-spot position on
- Heat transfer efficacy
- Maximal chip temperature
- Temperature homogeneity



-> Guidelines for chip architecture and integrated cooling design

Enhanced Cooling Performance

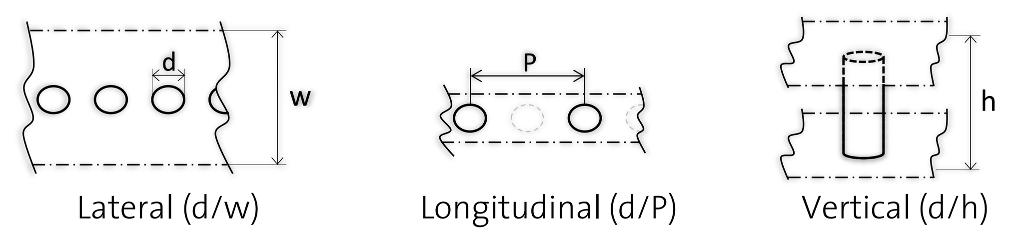


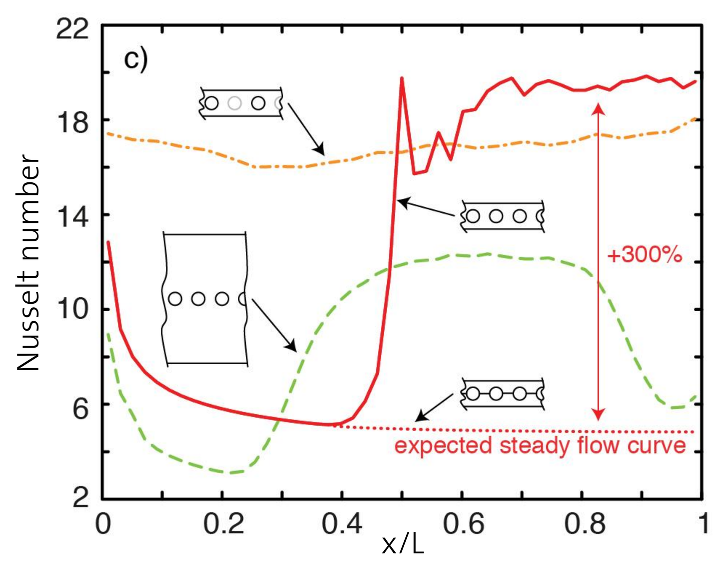
- Re < Re$_{crit}$: steady recirculation zones formed between the micropin fins
- Re > Re$_{crit}$: increased pressure drop and vortex-induced flow fluctuations in the kHz-range

-> disappearance of steady liquid hotspots enhanced the cooling performance up to 190%

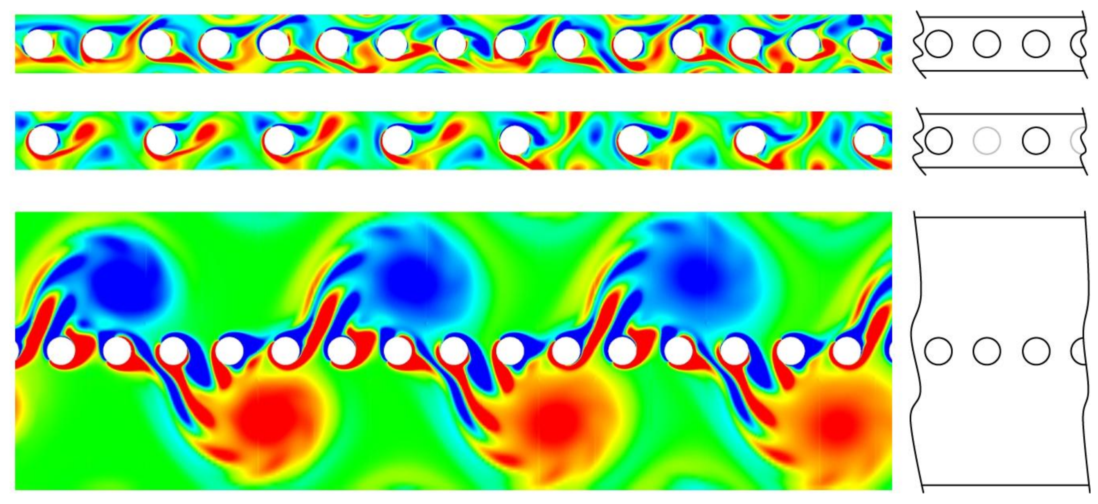
Confined Vortex Shedding

a) Types of confinement:

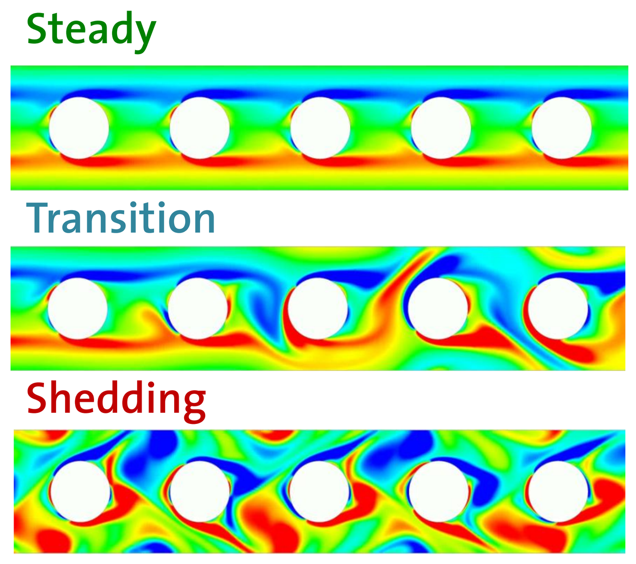




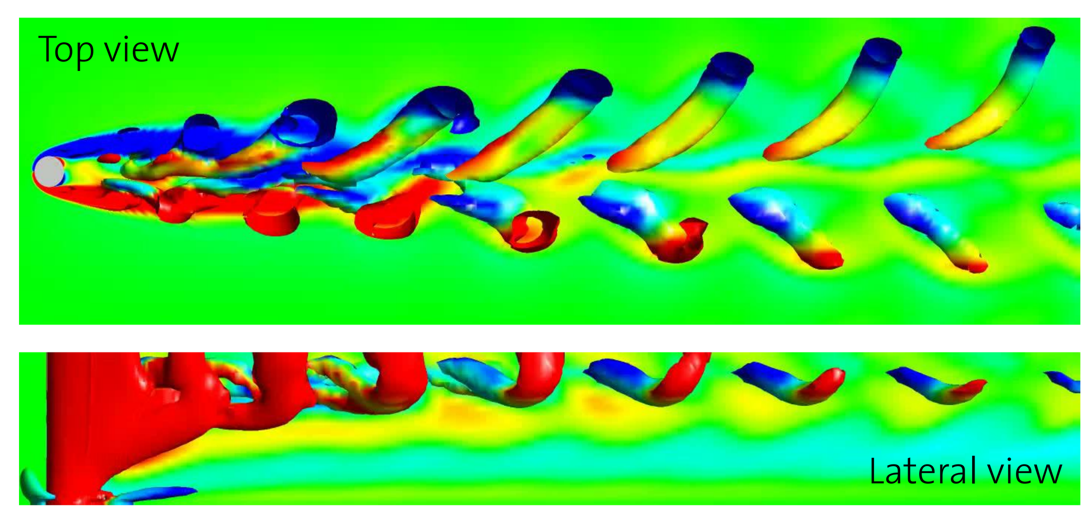
b) 300% heat transfer enhancement!



c) Laterally and longitudinally confined row of pins
-> collaborative effect of multiple pins



d) Regimes identification



e) Vertically confined pin
-> 3D vortical structures & endwall effect

Publications

- Renfer et al., *Experimental investigation into vortex structure and pressure drop across microcavities in 3D integrated electronics*, Experiments in Fluids (2011)
- Renfer et al., *Vortex shedding from confined micropin fin arrays*, Microfluidics and Nanofluidics (2012)
- Renfer et al., *Microvortex-enhanced heat transfer in 3D-integrated liquid cooling of electronic chip stacks*, International Journal of Heat and Mass Transfer (accepted for publication, 2013)
- Alfieri et al., *3D integrated water cooling of a composite multilayer stack of chips*, Journal of Heat Transfer (2010)
- Alfieri et al., *On the significance of developing boundary layers in integrated water cooled 3D chip stacks*, International Journal of Heat and Mass Transfer (2012)
- Alfieri et al., *Computational modeling of hot-spot identification and control in 3D stacked chips with integrated cooling*, Numerical Heat Transfer; Part A: Applications (accepted for publication, 2013)
- Alfieri et al., *Vortex shedding from confined cylinders and its implications on water cooled 3D electronic chips*, International Journal of Heat and Fluid Flow (submitted for publication, 2013)