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True Fractional-N dividers based on Injection Locking for low noise transmitters

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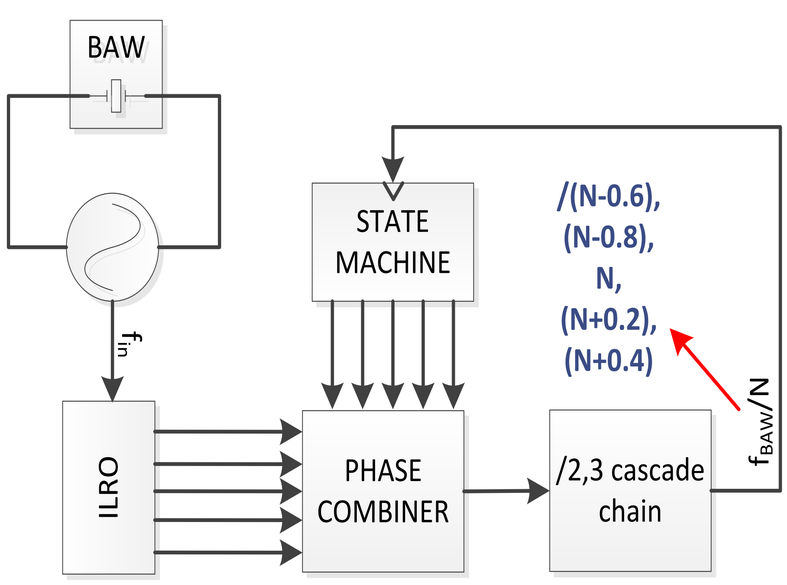
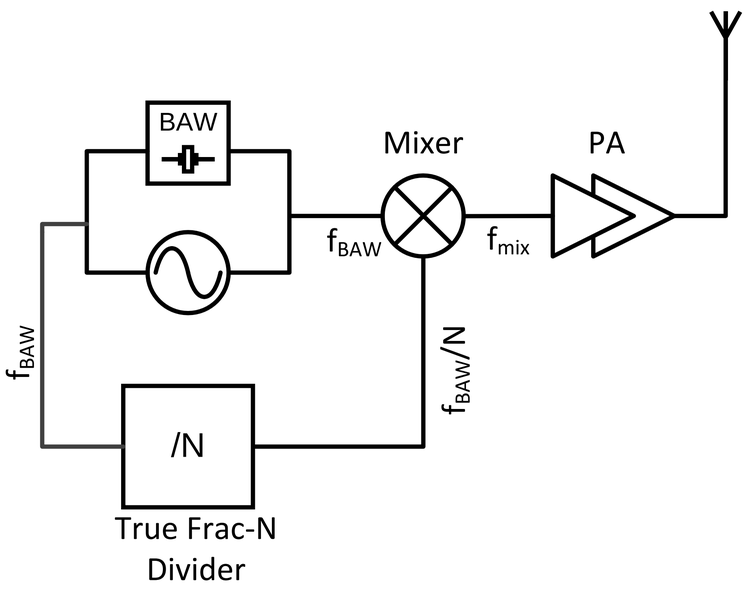
A true fractional dynamic divider using the principle of injection locking has been designed. The design of such divider is constrained primarily by the speed and the driving strength of the transistors, especially at 2.4 GHz which is the working frequency of the target application. This divider has been used instead of a conventional multi-modulus divider in a classical fractional-N PLL architecture with the aim of quantization noise reduction. Also, by combining the VCO and divider, a GFSK based direct modulation transmitter covering the 2.4-2.48 GHz ISM band has been designed and integrated in 65 nm technology.

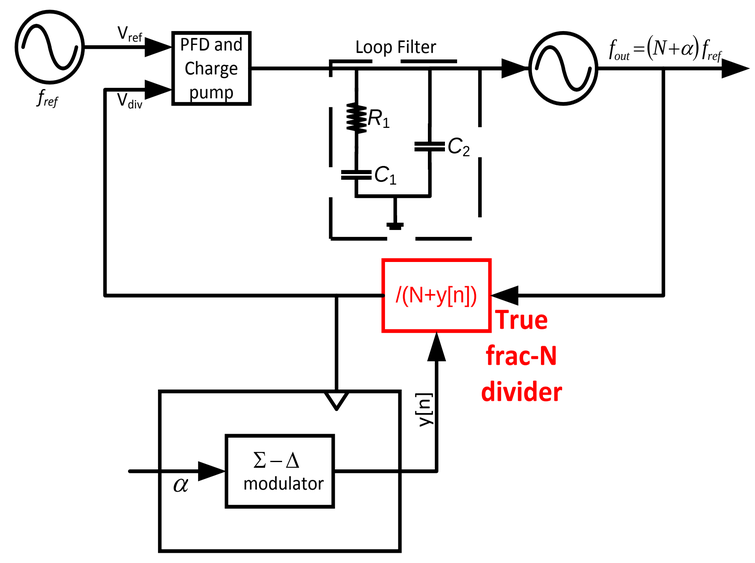
True Fractional-N dividers



TRUE FRACTIONAL-N DIVIDER



DIRECT MODULATION TRANSMITTER



CLASSICAL FRACTIONAL-N PLL WITH THE TRUE FRACTIONAL-N DIVIDER

TRUE FRACTIONAL-N DIVIDER

- Based on the principle of injection locking to the BAW oscillator to produce the required phases.
- State machine produces the necessary select signals.
- Phase combiner output fed to the programmable divider cascade.
- Advantage: Injection locked ring oscillator has the same phase noise performance as the BAW oscillator.

DIRECT MODULATION TRANSMITTER

- BAW based oscillator used to generate the reference – input to the true fractional-N divider.
- True frac-N divider used to choose the channel for addressing.
- Output of the BAW mixed with the divider signal to generate the required frequency. $f_{mix} = f_{BAW}\left(1+\frac{1}{N}\right)$
- Modulation performed by tuning the BAW.
- Tuning required on the BAW to cover the whole band is reduced by a factor *'k'* (k -division step size) compared to integer divider.

APPLICATION OF THE DIVIDER IN A FRACTIONAL-N PLL

- Quantization noise of the Sigma Delta modulator is one of the contributors to the noise at the output of the PLL.
- Phase noise due to the SDM (sigma delta mod)

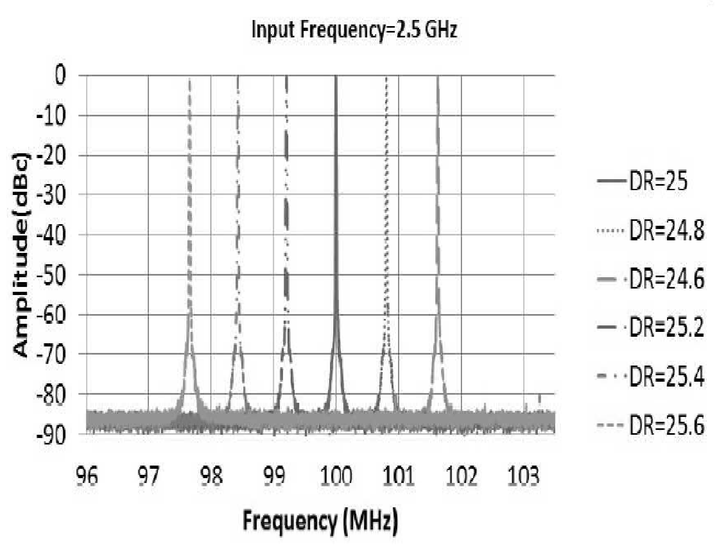
$$PN(f)[dBc/Hz] = 10\log\left\{\frac{\Delta^2 \cdot 4\pi^2}{12 f_r}\cdot\left[2\sin\left(\frac{\pi f}{f_r}\right)\right]^{2(m-1)}\right\}$$

- Δ → Step size of the divider.
- If Δ=0.2, the noise at the output of the PLL decreases by 14 dB (20 log Δ).

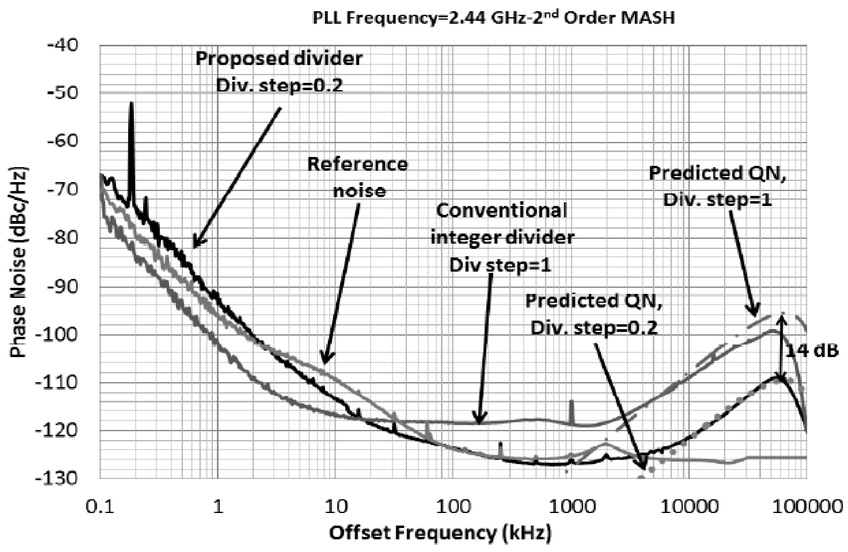
Conclusions

Parameter	[8]	[5]	This work
PLL Freq. range	0.97-1.96 GHz	0.8-3.8 GHz	2-2.6 GHz
Div. ratio range	36-83.5	30.5-510.5	8-31.4
Division Step	0.5	0.5	0.2
QN reduction	6 dB	6 dB	14 dB
Power dissip.	14 mA@1.8 V	5 mA@1.8 V	0.85 mA@1.1 V
Technology	180 nm	180 nm	65 nm

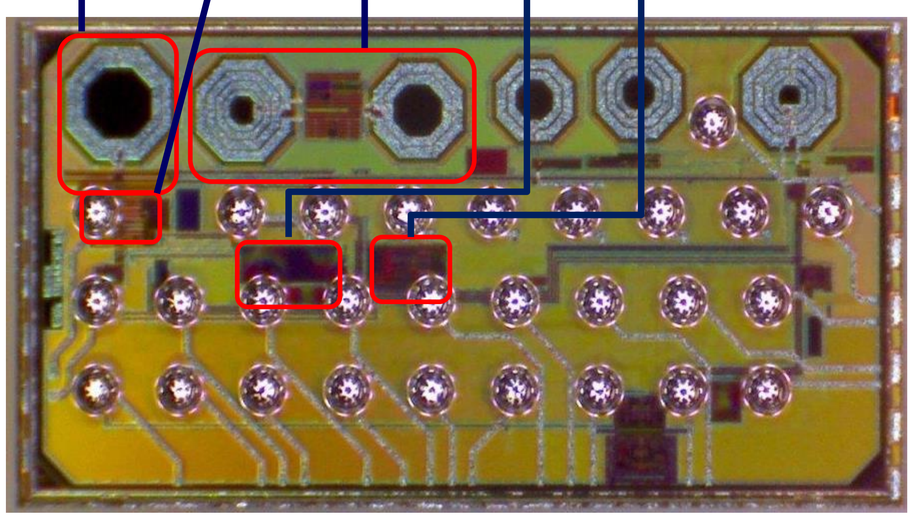
COMPARISON OF PERFORMANCE BETWEEN THIS WORK AND LITERATURE



DIVIDER OUTPUT SPECTRUM SHOWING DIVISION RATIOS FROM 24.6 TO 25.6



PHASE NOISE AT THE OUTPUT OF THE DIVIDER



MICROPHOTOGRAPH OF THE TRANSMITTER SYSTEM SHOWING THE TRUE FRACTIONAL-N DIVIDER

Conclusions

A true fractional-N divider which is based on the principle of injection locking to a BAW oscillator has been demonstrated in this work. The advantage of injection locking is that the phase noise of the divider closely follows the BAW oscillator. The power consumption of this divider is around 860 µW at 1.08V supply. This true fractional-N divider is used in a fractional-N PLL, where it serves to reduce the quantization noise arising out of the Sigma-Delta modulator by a factor *20 log* Δ, where Δ is the minimum achievable division step size (0.2 in this case). Furthermore, this divider has been employed in a direct modulation transmitter employing GFSK modulation.

References:

[5] Jing Jin; Xiaoming Liu; Tingting Mo; Jianjun Zhou, "Quantization Noise Suppression in Fractional-N PLLs Utilizing Glitch-Free Phase Switching Multi-Modulus Frequency Divider," Circuits and Systems I: Regular Papers, IEEE Transactions on , vol.59, no.5, pp.926-937, May 2012.

[8] L. Lu, Z. Gong, Y. Liao, H. Min, and Z. Tang, "A 975-to-1960 MHz fast-locking fractional-N synthesizer with adaptive bandwidth control and 4/4.5 prescaler for digital TV tuners," Proc. ISSCC Dig. Tech. Papers, Feb. 2009, pp. 396-397.