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PlaCiTUS RTD 2010

FNSNF

A DC-Connectable Multi-Channel Biomedical Data Acquisition ASIC

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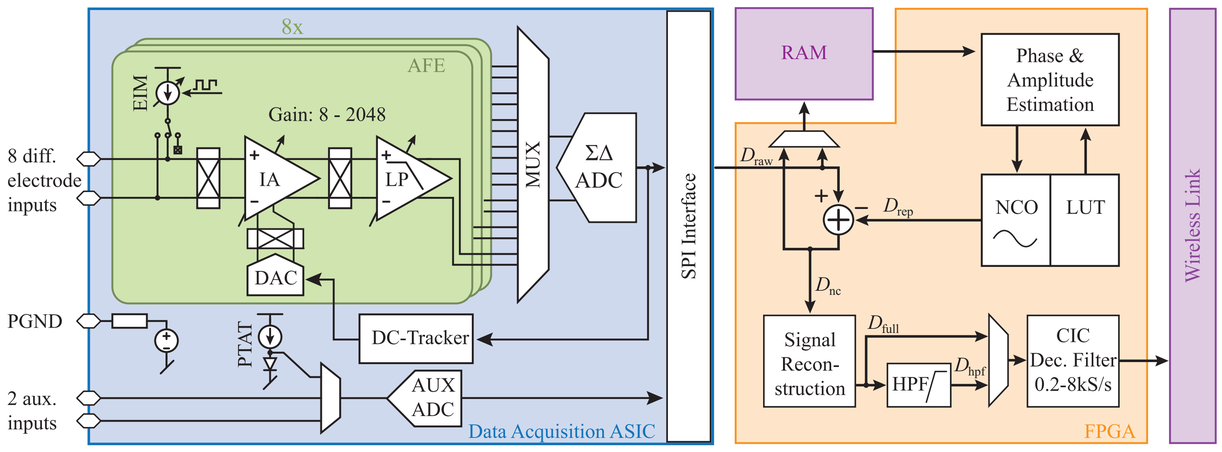
Abstract – We present an 8-channel biomedical data acquisition ASIC achieving 108dB of dynamic range (DR). Each channel includes a 13bit DAC to compensate differential input offset of up to ±300mV, preventing saturation of the high-gain instrumentation amplifier. Chopper stabilization and DAC-noise low-pass filtering lead to an input-referred noise of 0.8μV_{RMS}. Data processing algorithms, implemented on an FPGA, are employed to remove artifacts due to sudden DAC-switching and to cancel 50/60Hz mains interference including its harmonics. The chip is fabricated in 130nm CMOS, occupying an active area of 2.2mm² and consuming 15mW from 1.2V and 3.3V supplies.

1. System Overview



System breakdown

- ❑ Data Acquisition ASIC
  - ECG/EEG signals acquisition
  - Electrode impedance meas.
  - Temperature sensor
- ❑ Xilinx Spartan 6 FPGA
  - Controlling
  - Signal processing
  - Bluetooth connectivity to a Smartphone

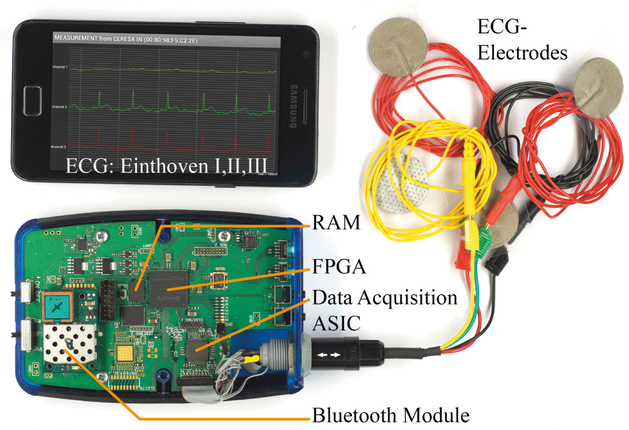


Fig. 1: System block diagram (top) and prototype (bottom).

2. Data Acquisition ASIC

Main features

- ❑ 130nm CMOS
- ❑ 2.19mm² area
- ❑ 8 electrode channels
- ❑ 2 aux. channels
- ❑ 1.2V & 3.3V supply
- ❑ 15mW max. power

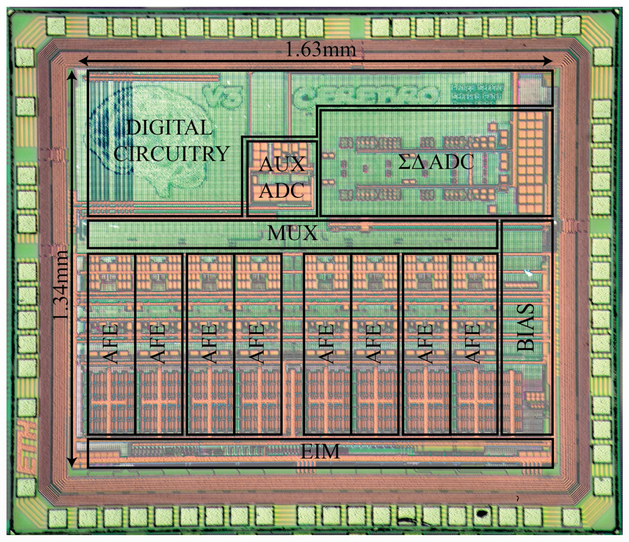


Fig. 2: Chip micrograph.

3. Analogue Front-End

- ❑ Chopper-stabilized IA [3]
- ❑ 3.2kHz low-pass filter
- ❑ ±300mV electrodes offset compensation DAC
- ❑ 8-channels MUX
- ❑ 82dB SNR (13.3 ENOB) ΣΔ ADC
- ❑ 8kS/s max. sampling rate

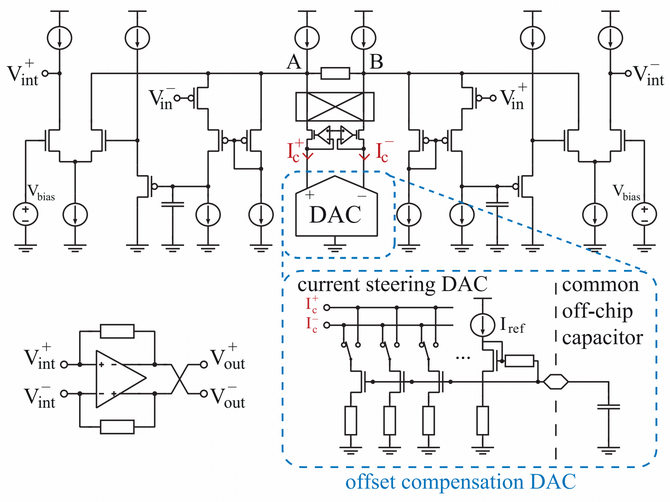


Fig. 3: Current balancing instrumentation amplifier (IA).

4. Digital Data Processing

- ❑ Mains interference cancellation by subtraction of a noise replica
- ❑ Power line harmonics removal
- ❑ Optional high-pass filtering
- ❑ Reconfigurable decimation

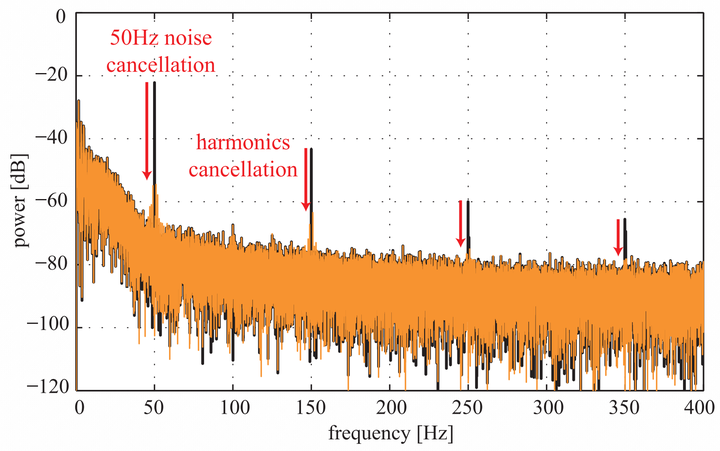


Fig. 4: Measured spectrum of an ECG signal before (black) and after signal processing (orange).

5. Measurement Results

- ❑ Low IR noise of 0.82 μV_{RMS}
- ❑ 107dB max. DR due to compensation DAC
- ❑ Moderate impact of DAC on noise performance
- ❑ High CMRR (101dB) and input impedance (235MΩ)

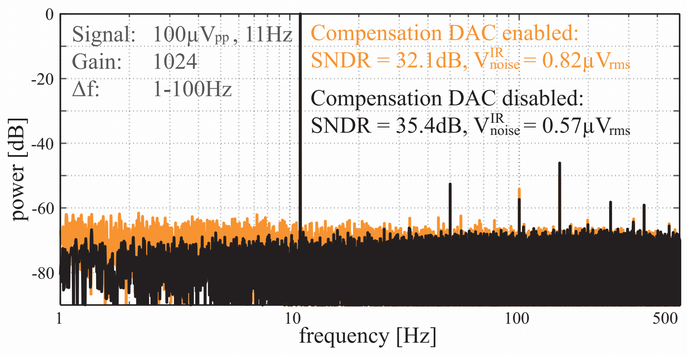


Fig. 5: Measured output spectrum of an electrode channel for an applied 100μV_{pp} sinusoidal test signal with compensation DAC enabled (orange) and disabled (black).

6. Performance Summary

Analog. Bandwidth:	3.2kHz	Sample Rate:	8kS/s
Tolerated Offset:	±300mV	Max. DR[a]:	107.6dB
Max. Input Swing[b]:	42mV	Max. SFDR[b]:	66dB
CMRR:	101.0dB	Inp. Impedance:	235MΩ
IR Noise:	82nV/√Hz	RMS IR Noise[c]:	0.82μV

a. incl. DC tracking. b. for a constant offset. c. 1-100Hz signal bandwidth.

References:

[1] R. Yazicioglu et al., "A 200 μW Eight-Channel EEG Acquisition ASIC for Ambulatory EEG Systems," *JSSCC*, vol.43, no.12, pp.3025-3038, Dec. 2008.

[2] H. Kyong, N. Verma, "A 1.2–0.55V general-purpose biomedical processor with configurable machine-learning accelerators for high-order, patient-adaptive monitoring," *Proc. ESSCIRC*, Sept. 2012, pp.285,288.

[3] Q. Huang, C. Menolfi, "A 200 nV offset 6.5 nV/√Hz noise PSD 5.6 kHz chopper instrumentation amplifier in 1μm digital CMOS," *ISSCC*, pp.362-363, Feb. 2001.