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QCrypt RTD 2010

FNSNF

Challenge of Designing PCBs with complex FPGA and very high speed links

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Challenge of Designing Complex PCBs

26 Cu Layers PCB
High power supplies - up to 40 A
26 power supplies, 18 internal planes
Thick board versus Thin vias
Backdrilled vias
Routing FPGA with 2'000 pins
Very high speed signals up to 10 GHz
Controlled-impedance differential pairs

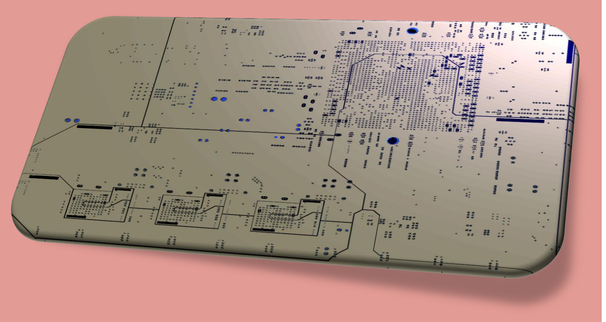
Power distribution

Layer usage - Ideal

- Thick copper
- Thin prepreg: high capacitance
- Many short vias, vias in pads

Layer usage - Reality

- Symetric stackup: high current on top
- Thick copper – thick prepreg: filled planes for thinner prepreg

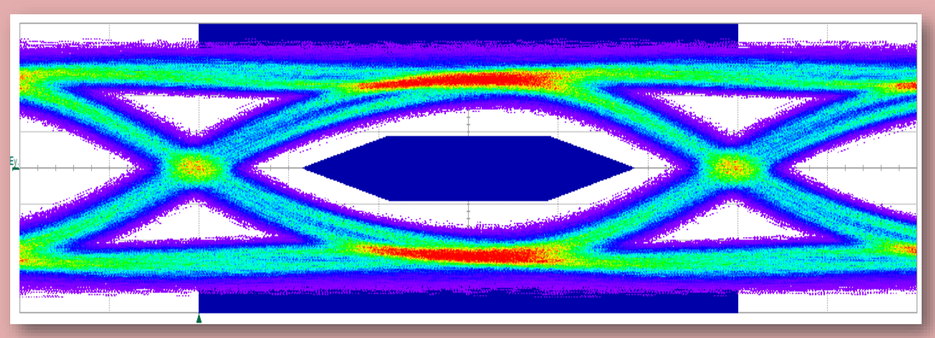


High speed signaling

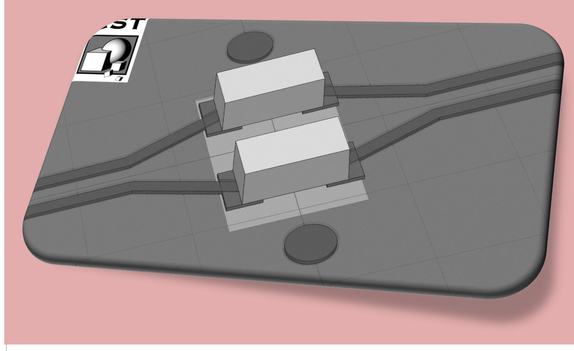
PCB V1 Eye Measurements

Eye measurement of a SFP+ transceiver

The measurement of the eye is made using a SFP+/SMA adapter plugged to a SFP+ connector of the QCrypt board and connected to two SMA inputs of the oscilloscope.



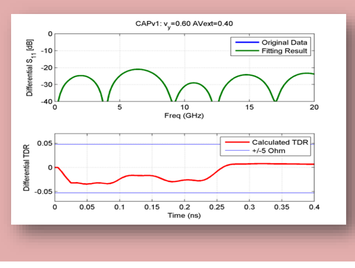
PCB V2 3D Simulations



Simulation of two capacitors in a differential high-speed connection

The capacitors are simulated as metal bricks. The curves show the optimal simulation result for the structure.

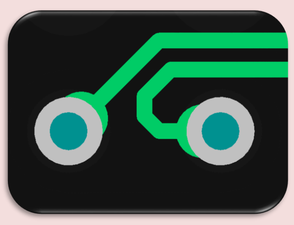
The green curve is the reflected energy. The red curve corresponds to a TDR measurement indicating the impedance deviation over the length of the line.

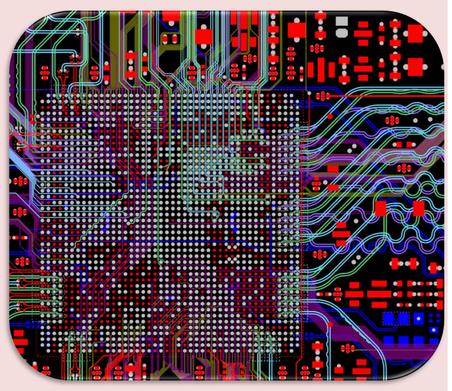


The 3D simulations have been carried on the CST STUDIO SUITE™.

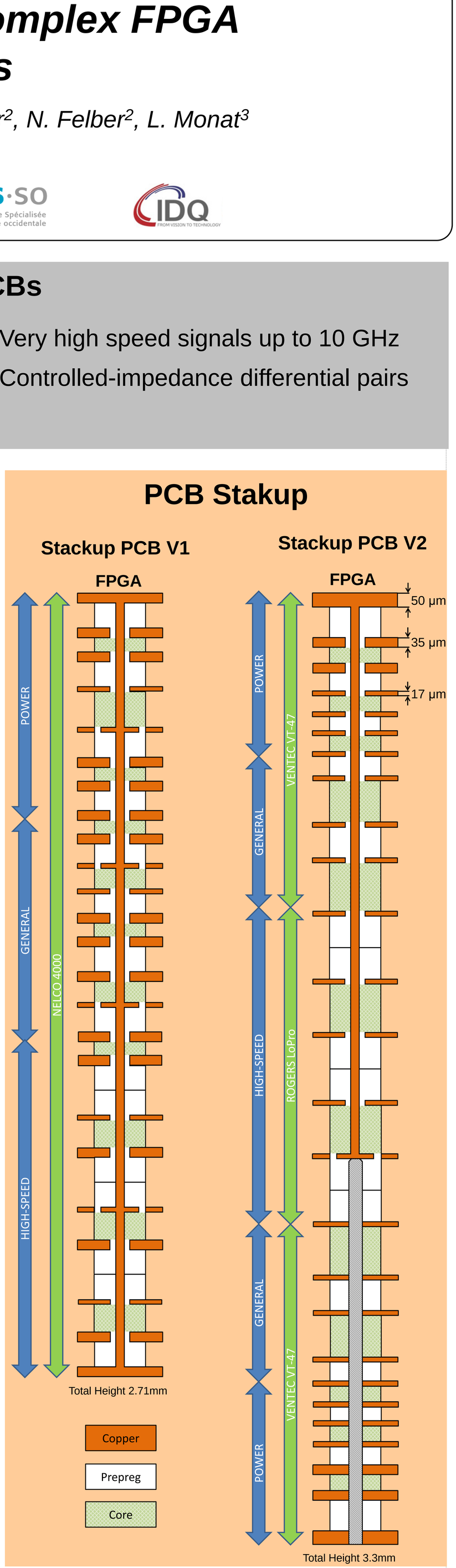
High density routing

- Narrow and wide differential lines
- Phase- and length-matched traces
- Via in pads
- Minimal vias of type snowman
- Space sharing of traces and decaps
- Clearance vs. low-res power planes





PCB Stakup



History of PCB design and fabrication

PCB V1
PHOTOCHEMIE †
24 Cu Layers, asymetric
≥ 0.2mm Vias

PCB V2
WIKO †
26 Cu Layers, symetric
≥ 0.22mm Vias

Evaluation of more than 14 companies:
None without Redesign !

→

PCB V2
MicroPCB ✓
26 Cu Layers, symetric
≥ 0.25mm Vias

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