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A CMOS-Compatible Chip-to-Chip Integration Platform

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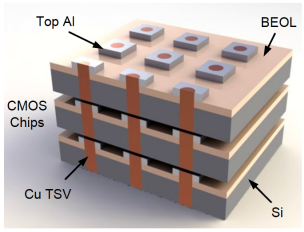
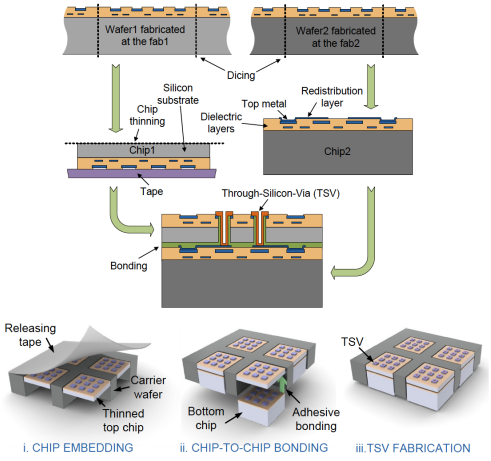
INTRODUCTION

In this paper, a CMOS-compatible chip-to-chip (C2C) 3D integration platform is presented. The developed technology allows reconstituting a wafer from diced and thinned chips. Then, chip-to-chip bonding and TSV fabrication steps are accomplished in wafer-level. Two dummy chips are successfully bonded, and TSVs with parylene sidewall passivation and electroplated Cu metallization are fabricated. The resistance measurements demonstrate average TSV resistance of 0.5Ω. The proposed technique introduces a simple and low-cost solution not only for 3D integration technology but also for applications involving CMOS post-processing in general.



Die-Level 3D Integration

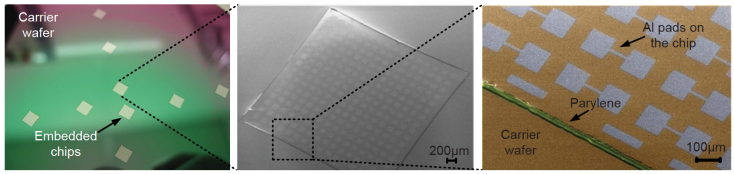
- **Back-to-face type via-last C2C integration process. Identical or heterogeneous chips can be post processed after dicing. The TSVs are fabricated after alignment and bonding.**



- **Proposed 3D integration process comprising wafer reconstitution, bonding, and TSV fabrication.**

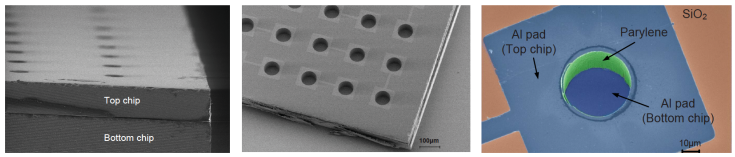
Fabricated Devices

Chip Embedding



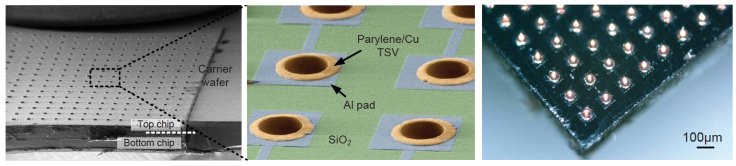
- Diced chips are thinned down to 50µm and embedded into a carrier wafer by parylene deposition.

Bonding and Etching



- C2C Bonding
- Al, Dielectric, and Si Etching
- Sidewall passivation

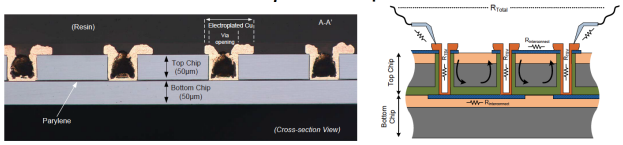
Electroplating



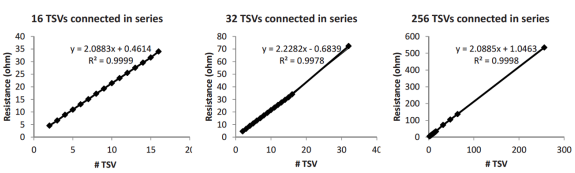
- Seed layer deposition, dry-film lithography, and Cu electroplating.
- Chip releasing

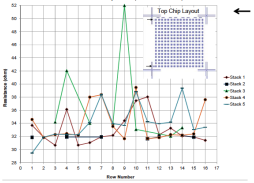
Resistance Measurements

- **Cross-section view of the two 50µm thick chips connected with Cu TSVs.**



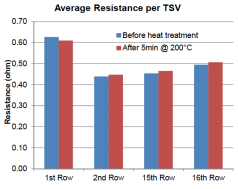
Daisy-Chain Measurements





← 1280 TSVs from 5 different chip stacks are measured, and just 10 defects are detected.

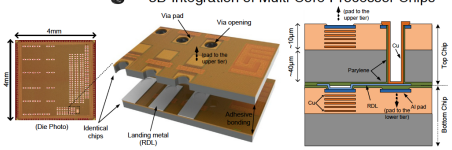
0.5Ω of TSV resistance is measured. →



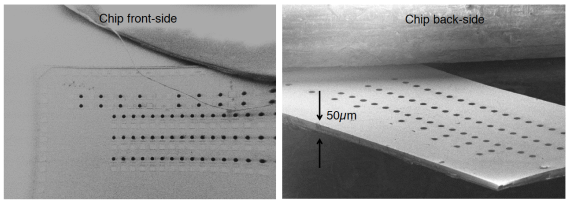
Microprocessor Stacking

- Each chip comprises four 32-bit LEON3 processors, memory, and 3D Network-on-Chip.
- 120 TSVs: 54 Power TSVs and 66 Signal TSVs

3D Integration of Multi-Core Processor Chips



Top Chip
Grinding down to 50µm
Chip-level photolithography
Al, dielectric, and Si etching



Bottom Chip
Surface passivation
Passivation etching
Redistribution layer patterning