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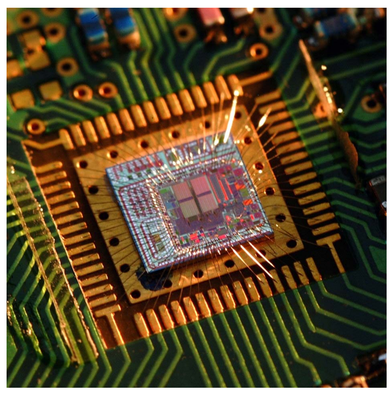


Sub- and near-threshold design for nano-Watt scale integrated circuit (IC)

Marc Pons, Daniel Séverac, Christian Piguet

CSEM SA, Switzerland

:: csem

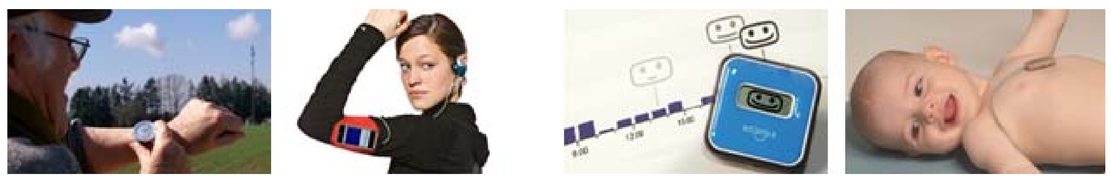
info@csem.ch www.csem.ch

Low-power applications (including wireless sensor networks, RFID or watches) are always looking for solutions to lower the power consumption despite supporting additional features. One effective way of reducing the power consumption is by reducing the supply voltage. Transistors operate in two distinct modes depending on the supply voltage level: in super-threshold mode (most commonly used), the supply voltage is well above the threshold voltage of the transistor that is then a nearly perfect switch; in sub-threshold mode, the supply voltage is below that threshold and the transistor is a less perfect switch. In the IcySoC project, we develop a technique to work with transistors supplied at a sub-threshold voltage, which minimizes their power consumption but reduces their speed. When faster switching is required, a near-threshold supply voltage offers a good compromise between power consumption and speed.

Motivation: ultra-low power IC

Examples of ultra-low power applications:

- Wireless sensor networks, watches, RFID, ECG…



Needs for reduced power consumption:

- Longer battery life
- Miniaturization of battery
- Reduced battery weight
- Support more functionalities with same energy
- Energy autonomy through energy harvesting

CMOS Sub-threshold Design

- Many ultra-low power techniques are based on power supply voltage (V_{DD}) reduction

Power consumption	V_{DD} dependance
Dynamic (P_{dyn})	V_{DD}^2
Static (P_{stat})	V_{DD}

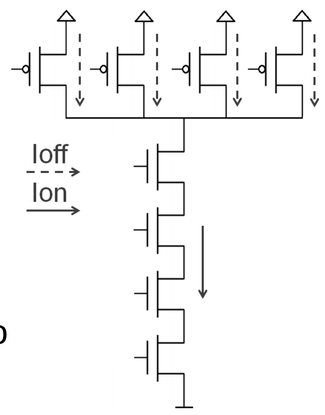
- Sub-threshold operation: $V_{DD} < V_{TH}$ (threshold voltage of transistors)

Benefits:

- P_{stat} and P_{dyn} reduction

Challenges:

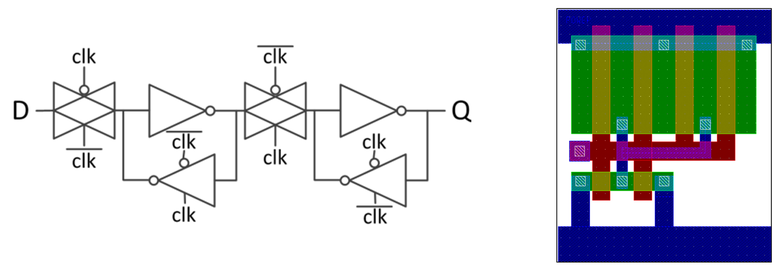
- Working with weak (less perfect) transistors
- Increased sensitivity to V_{TH} variations due to foundry variability



Sub- and near-threshold building bricks for integrated circuits

STANDARD CELL DESIGN

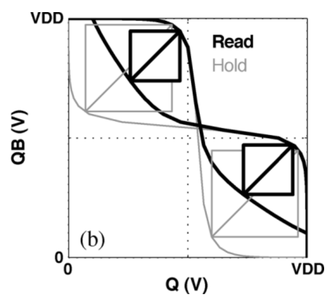
- Methodology to adapt existing standard cell libraries to subthreshold operation
  - Threshold voltage selection
  - Supply voltage selection
  - Sizing methodology of transistors
- The above are technology dependent. Three technologies are targeted:
  - Bulk CMOS in 180 nm and 65 nm
  - FDSOI in 28 nm



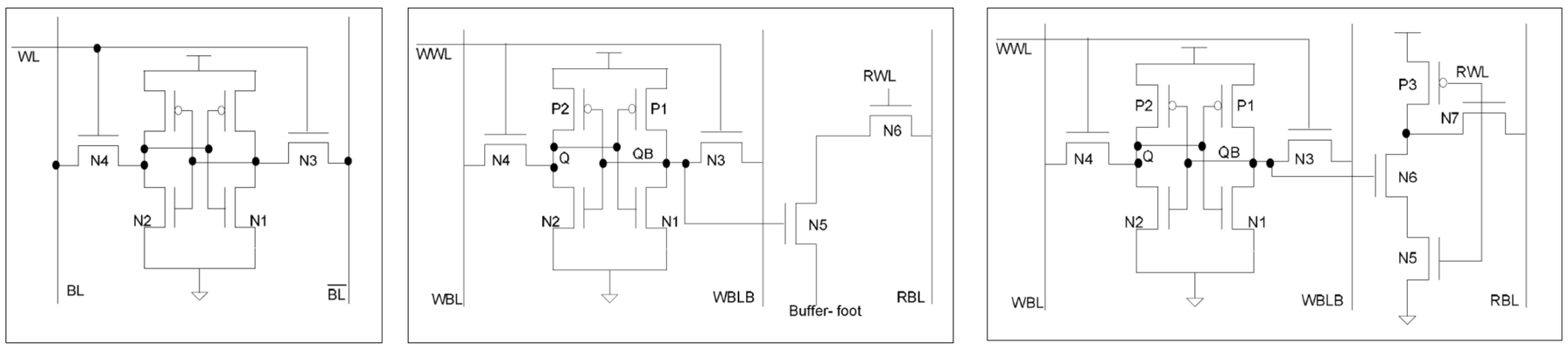
Standard cell (schematic and layout)

SRAM MEMORY DESIGN

- Current state-of-the-art: 6-Transistor (6T) bit-cell operates down to 0.7 V
- Step 1: Resizing of 6T bit-cell to operate at lower voltage
- Step 2: If no 6T solution found, consider 8T-10T bit-cells for sub-threshold operation
- Step 3: Analyze robustness (Process-Voltage-Temperature variations, Monte Carlo analysis, evaluation of Static Noise Margin)



Butterfly graph for Static Noise Margin



Architecture of SRAM bit-cells: 6T (left), 8T (center) and 10T (right)

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