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swiss scientific initiative in health / security / environment systems

IcySoC RTD 2013

FNSNF

IcySoC: Inexact Sub/Near-Threshold Systems for Ultra-Low-Power Devices

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CSEM, EPFL ICLAB, ETHZ, EPFL TCL, EM Microelectronics

PROJECT: This nano-tera project, called IcySoC, combines several contributions, i.e. a multi-processor platform, inexact arithmetic and sub/near-threshold design.

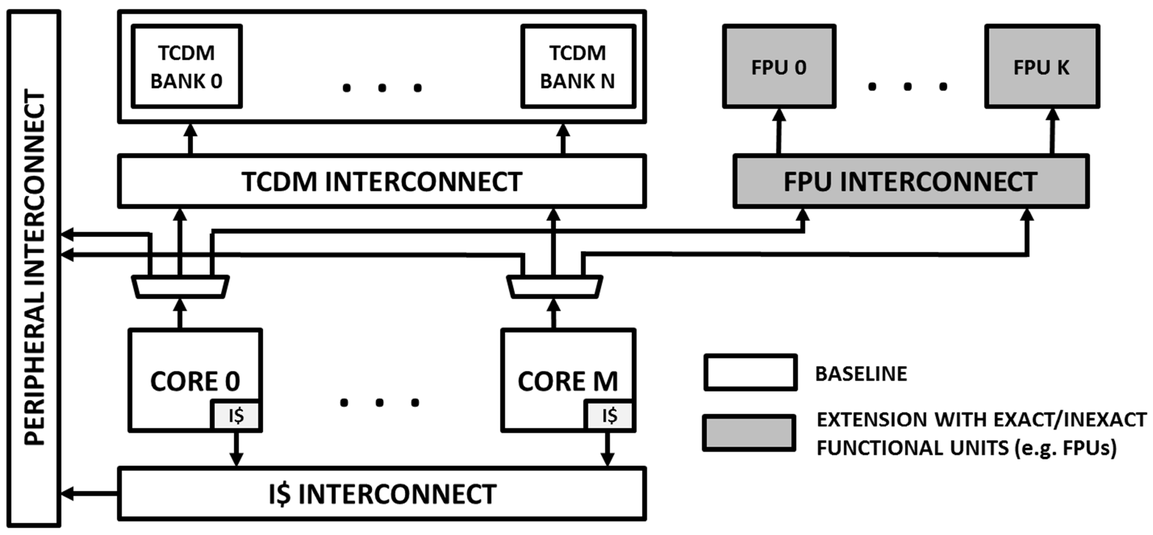
PLATFORM: The platform will comprise several processor cores connected through a low-latency on-chip interconnect. The latter will connect many hardware accelerators for dedicated high intensive computation loads.

GOOD ENOUGH: Some of these accelerators will be designed as inexact arithmetic blocks, or good enough blocks. It means that for some applications (image processing, video, audio), small errors are not noticeable by the users. This first radical approach realizes parsimonious or “adequately engineered” designs that trade accuracy at the hardware level for significant gains in energy consumption, area, and speed.

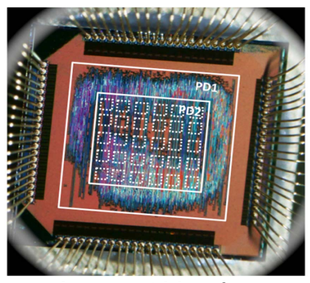
SUB/NEAR-THRESHOLD: The second approach based on sub/near-threshold design offers the minimal power or energy consumption at the cost of increased delay and power variations. We will push to the limit the supply voltage reduction by reaching the sub/near-threshold region of operation of transistors, thus supplying the circuits at a voltage equal or lower than the threshold voltage of transistors and maximizing the power reduction due to voltage tuning.

APPLICATIONS: A large class of energy constrained systems, particularly in the domain of embedded portable multimedia and in domains of budding interest such as recognition, search and data mining, lend themselves readily for such a design philosophy. In fact, all of which can tolerate inaccuracies to varying extents or can synthesize accurate (or sufficient) information even from inaccurate computations.

MULTI-DISCIPLINE: platform, inexact and sub-T, DSP, algorithms, multimedia, but not too much to have the right distances between partners (each partner is capable of understanding what the other are doing)



Platform with inexact and sub/near-threshold accelerators

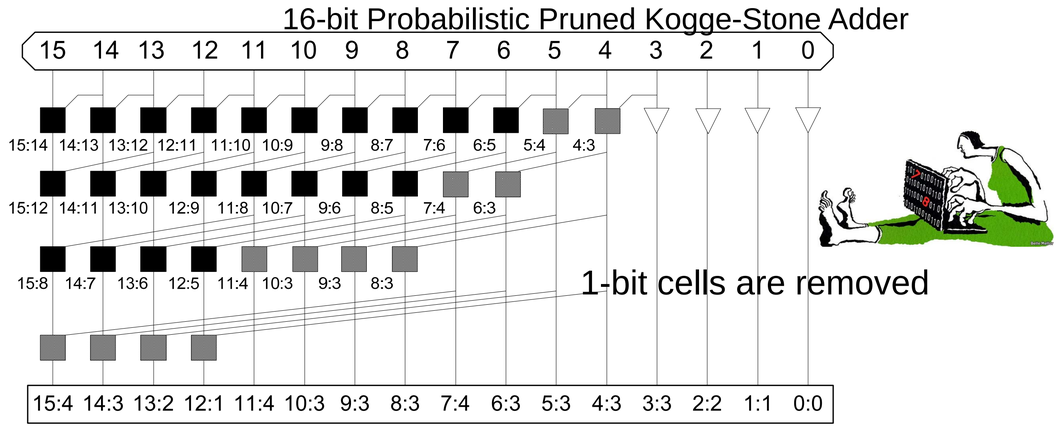


Inexact Hardware

The Economist, June 2nd-8th 2012

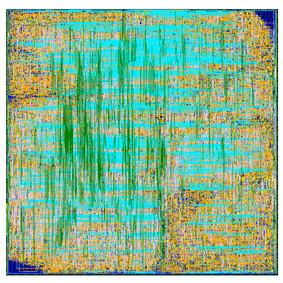
Oh, that’s near enough
Computing: Letting microchips make a few mistakes here and there could make them much faster and more energy-efficient

16-bit Probabilistic Pruned Kogge-Stone Adder



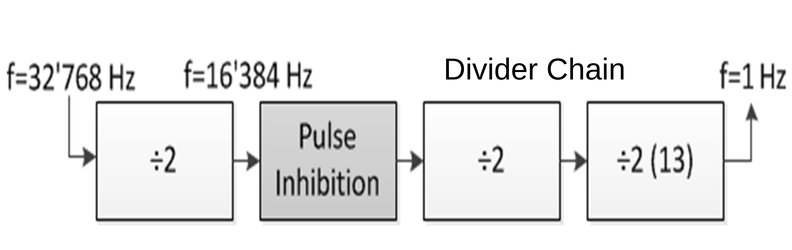
1-bit cells are removed

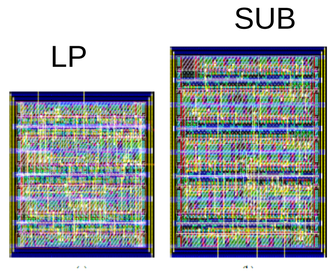
Sub-T icyflex2 processor core



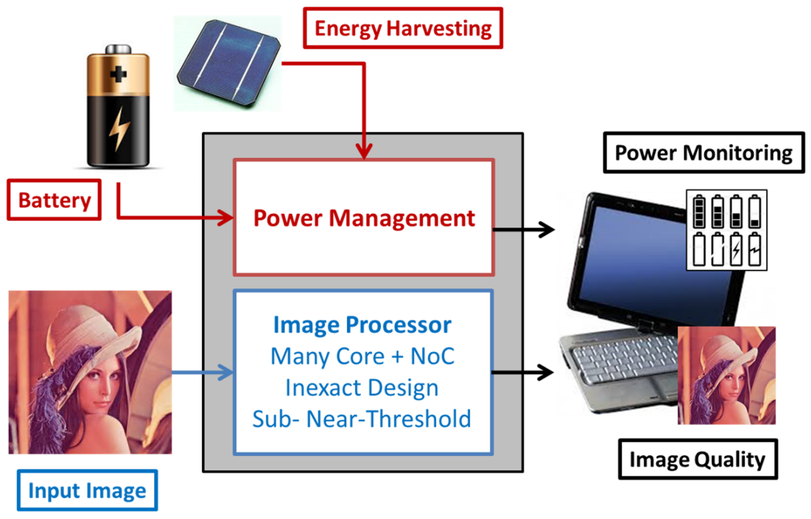
Divider Chain

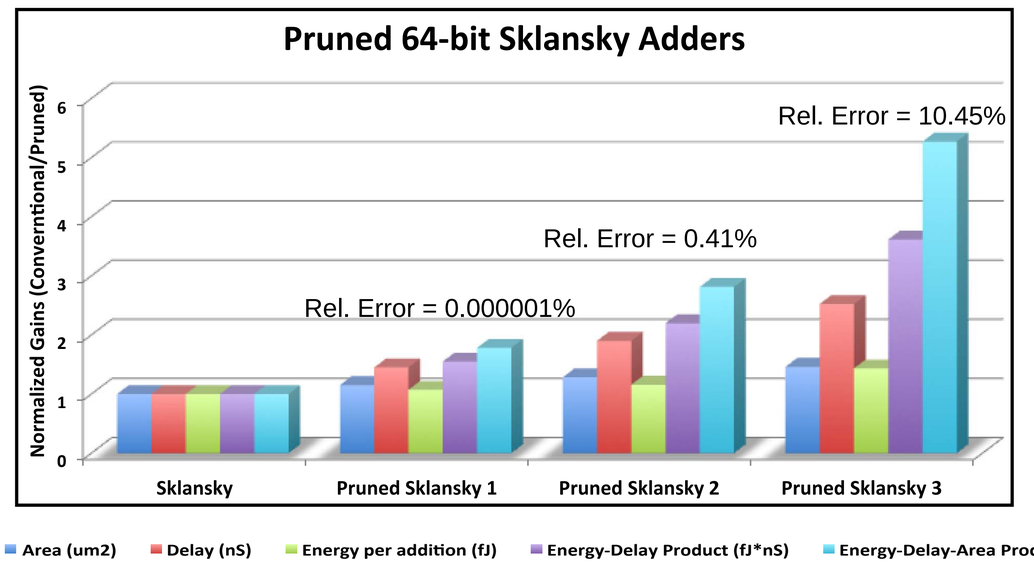
Library	Area	Frequency	Worst Case Power
LP 180 nm	1265 µm²	32 kHz	3.4nW/cycle @FF, 125°C (x11.6)
SUB 180 nm	1870 µm² (x1.5)	32 kHz	0.29nW/cycle @FF, 125°C





Sub/Near-Threshold





Great Synergy between:
- Platform
- Good enough circuits
- Sub/Near-Threshold

Other topics:
-VLSI circuits and DSP architectures for computing with unreliable silicon
- Algorithms to mitigate the impact of circuit misbehavior and delay variations