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Integration of WearMeSoc: The Wireless Health Monitoring Platform

ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich

S. Fateh, P. Schönle, P. Bunjaku, T. Burger, Q. Huang

Integrated Systems Laboratory – ETH Zürich

Abstract — Ageing population and high medical costs in industrialized nations in recent years demand for medical devices to keep up with the latest advances in microelectronics, and for the development of better and miniaturized health care for ambulatory environments. If no action is taken to prevent the increasing costs, healthcare might become unaffordable in the near future. Anyway, curing illnesses is more expensive than its prevention. Therefore, personalized and preventive monitoring healthcare is a necessity to reduce medical costs. People should be motivated to monitor their own health and they should get continuous feedback to improve their lifestyle. The aquisition of these biomedical signals require advanced technologies which are easy to use, cheap, and comfortable to wear. Integration of health monitoring platform in a single chip helps to shrink the size of the device while reducing power consumption. With the single chip biomedical platform also new medical research fields are enabled.

Surface EEG, ECG, EMG and other electrode based measurements are amongst the applications supported by the presented health monitoring platform. The heart of the platform is built by a highly optimized RISC CPU which is reponsible for a fluent operation of the platform (Figure 1, 2).

Flexible and modular hardware can be built by using microprocessors to control the underlying dedicated hardware on software basis. Within the WearMeSoc project, an open-source RISC microprocessor (see Figure 1) is optimized to operate low power which is fundamental in portable applications. Figure 2 shows the role of the RISC within the platform controlling all fundamental periphery responsible for data flow.

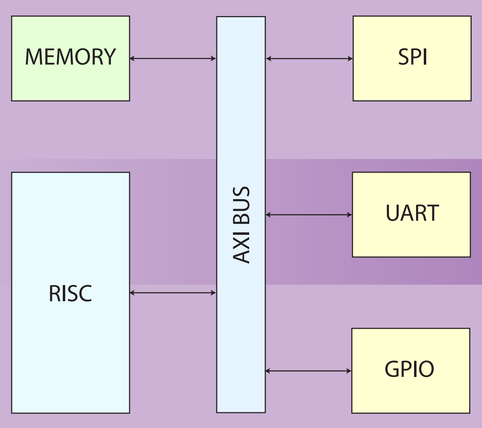

Figure 1: RISC microprocessor connected through an AXI AMBA BUS to its standard periphery, i.e., SPI, UART, GPIO.

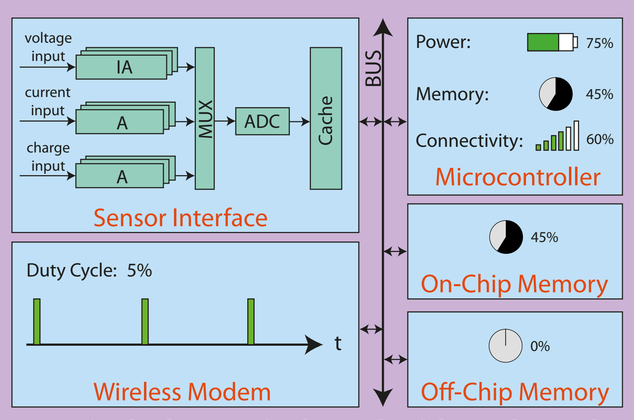

Figure 2: The data transfer duty cycle of the wireless modem needs to be regulated by the RISC CPU, which builds the power bottle-neck of the overall system.

The analog front-end planed to be integrated in the health-care monitoring platform is prototyped as a test chip on CMOS basis and is already in practical use (see Figures 3 and 4). However, the new platform is extended with electrical stimulation capabilities (as illustrated in Figure 5) which is necessary for certain biomedical applications, e.g., pulse-oximetry, which acquires biomedical signal through stimulation of LEDs.

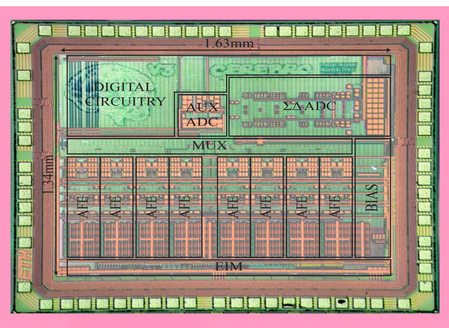

Figure 3: Chip micrograph of Cerebro.

The 8-channel biomedical data acquistion ASIC called Cerebro achieves a dynamic range of 108 dB with an input-referred noise of 0.8 µVrms for each channel (see Figure 3). The prototyped portable ECG/EEG device shown in Figure 4 is based on Cerebro, a Xilinx Spartan 6 FPGA for signal processing, and a Bluetooth module. Beside the current data acquistion system Cerebro, new data acquisition channels and actuators are designed as shown in Figure 5.

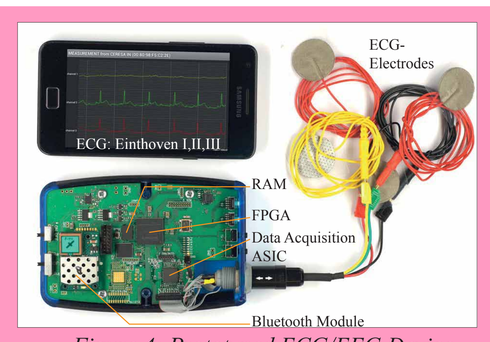

Figure 4: Prototyped ECG/EEG Device.

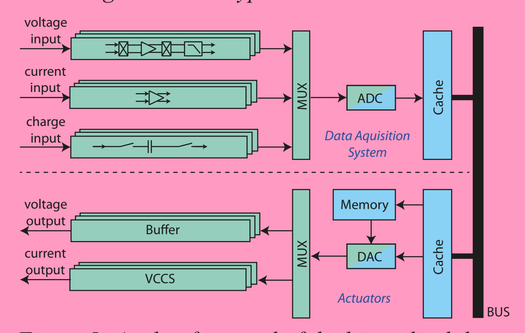

Figure 5: Analog front-end of the biomedical data acquisition platform.

The raw biomedical data needs to be processed by hardware accelerators before interpretation (see Figure 6, 7). A power-effient A/D converter architecture is also a necessity and for this reason, a self-calibrating SAR A/D converter is protyped in CMOS to achieve 13 bits of resolution (see Figure 8-10). The combination of the RISC CPU, low-noise analog front-end, hardware accelerators, and SAR ADC builds the single chip platform presented in Figure 11.

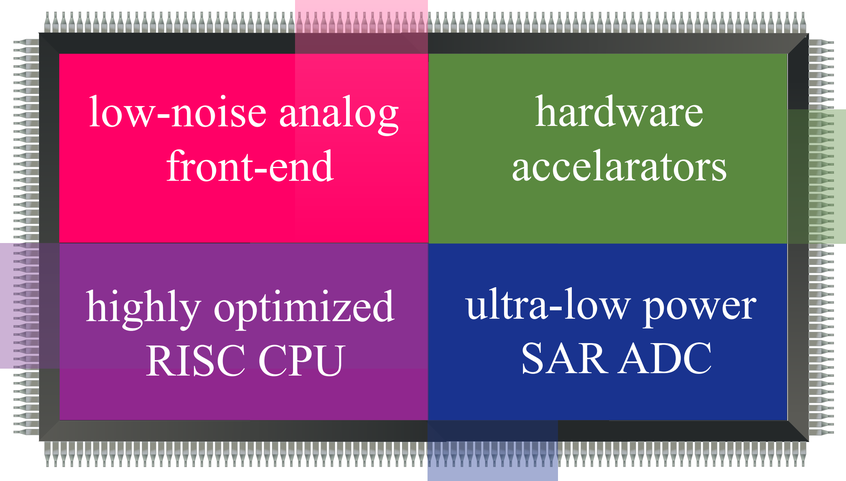

Figure 11: WearMeSoc - the single chip wireless health monitoring platform.

A fully integrated SAR ADC in 130 nm CMOS employing a non-uniform clocking scheme and an on-chip perturbation based start-up calibration to correct non-linearity introduced by the capacitor array is shown in Figure 8 and 9. The converter features 78 dB SNDR at 10 kS/s with OSR = 4, which makes it suitable for high resolution battery-powered biomedical applications (see Figure 10). The chip consumes 19 µW from a single 1.2 V supply. The performance summary is given in Table 1.

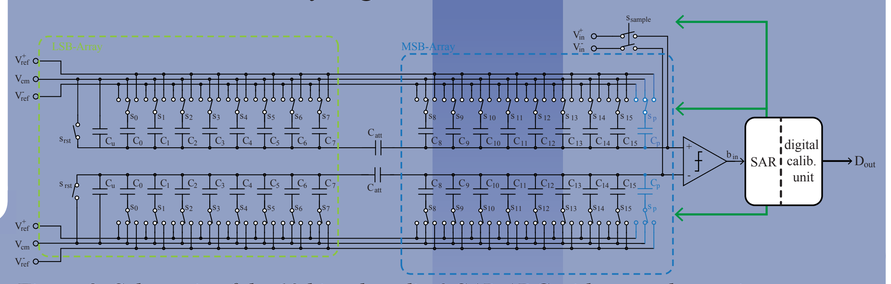

Figure 8: Schematic of the 13 bit sub-radix-2 SAR ADC with merged capacitor switching scheme.

Research and advances in digital signal processing with emphasis on biomedical applications reduces environmental interferences and improves interpretation capabilities of recorded raw biomedical data. As can be seen in Figure 6, hardware friendly algorithms can be derived and implemented supporting the reduction of environmental interferences. To shorten the time to market, a real-time development environment (see Figure 7) is built on the basis of a Xilinx Spartan 6 FPGA for the WearMeSoc project which improves the testability of the developed algorithms and ASICs, and improves the robustness of the system under real conditions. The digital hardware accelerators can be tested in combination with the RISC microprocessor which builds the controlling unit of the platform.

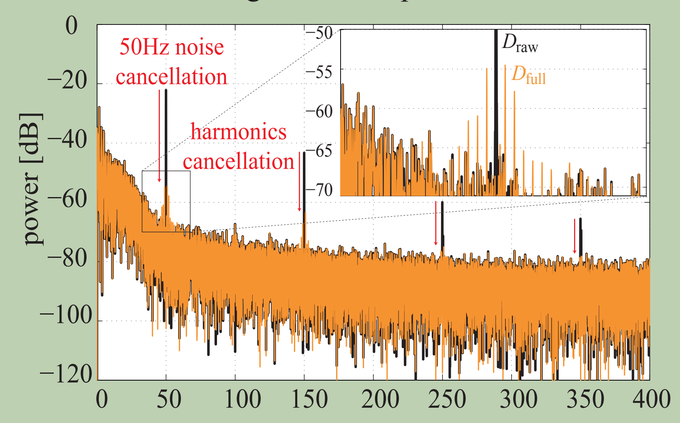

Figure 6: Measured spectrum of ECG before (black) and after digital signal processing (orange).

Figure 7: Real-time development environment.

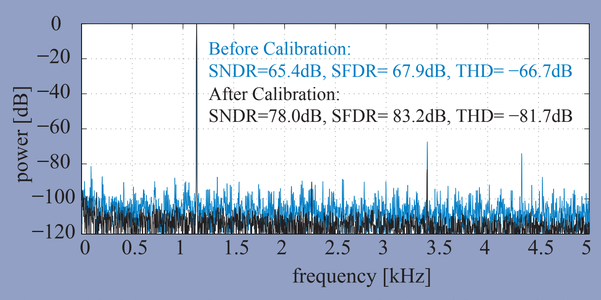

Figure 10: Measured output spectrum before (blue) and after (black) calibration at 10 kS/s with a 1.1 kHz input.

Sampling Rate	10 kS/s (OSR = 4)
Technology	130 nm CMOS
Peak SNR [dB]	80.3
SFDR [dB]	83.2
Peak SNDR [dB]	78
ENOB [bit]	12.7
Power [mW]	0.019
FOM[a] [fJ/conv]	294

[a] FOM = Power/ $2 \cdot BW \cdot 2^{ENOB}$

Table 1: ADC performance summary.

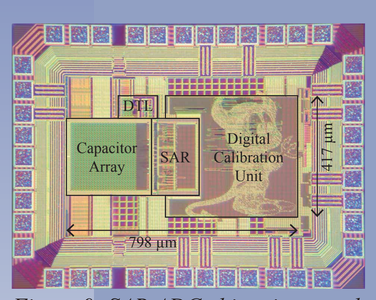

Figure 9: SAR ADC chip micrograph implemented in a 130 nm CMOS technology.