nano-tera.ch
swiss scientific initiative in health / security / environment systems

WearableMRI RTD 2013

FNSNF

An Integrated Receiver for MRI in 130nm CMOS

ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

B. Sporrer, L. Bettini, T. Burger, Q. Huang

Integrated Systems Laboratory – ETH Zurich

Wearable MRI

Abstract – In this work we present a CMOS receiver chain for MRI data acquisition. Integration allows for very small receiver board designs which are required for wearable MRI sensor arrays. The power consumption has been minimized in order to employ optical power transmission to supply the wearable device. The MRI signal has a bandwidth of up to 2 MHz, at RF frequencies ranging from 128MHz to 300MHz, and depending on the receiver coil, a peak input SNR which can be as high as 74dB. The direct conversion receiver needs therefore to fulfill very stringent requirements on linearity and dynamic range besides offering a very low NF. To guarantee fast and accurate image generation the whole integrated receiver chain shows a NF of only 1.4dB (at an input SNR of 74dB).

1. System Overview

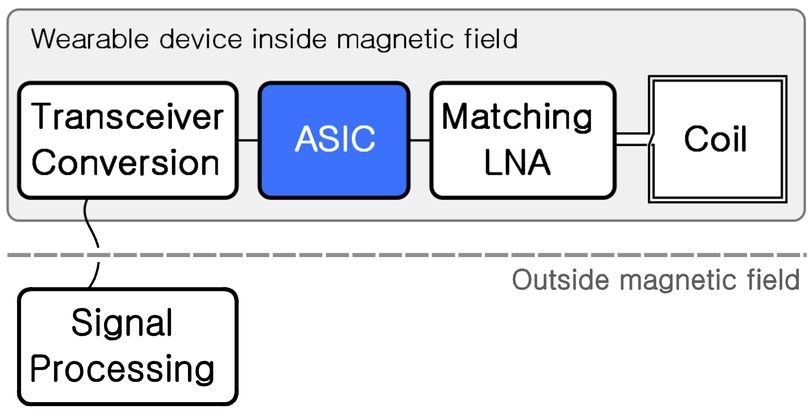

Fig. 1: Overview of the wearable MRI device, that will collect and digitize the measurement data within the magnetic field of the MRI scanner

2. CMOS Receiver

- ❑ **Programmable signal bandwidths up to 10MHz**
- ❑ **Very low Noise Figure of 1.4dB**
- ❑ **High dynamic range**
- ❑ **Adjustable Gain allows to reduce the NF even further**
- ❑ **Integration greatly reduces the part count on the wearable receiver board**

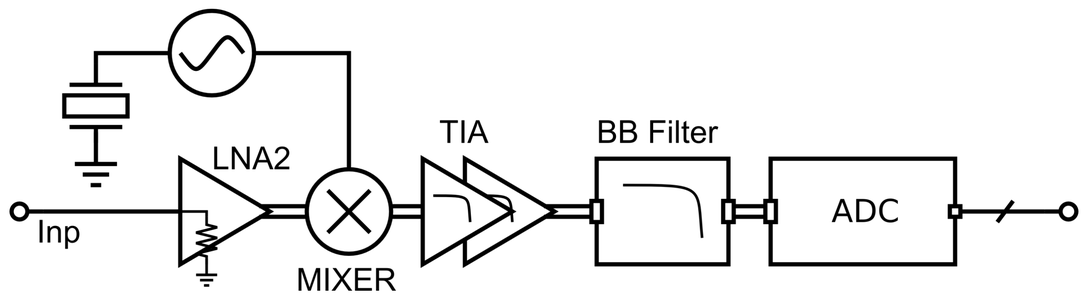

Fig. 2: Architecture of the reconfigurable receiver.

3. Analogue Front-End

- ❑ **Active balun LNA, matched to 50Ω (single-ended)**
- ❑ **High linearity mode available for LNA**
- ❑ **AC coupled passive mixer**
- ❑ **Low jitter fully-integrated PLL**
- ❑ **2nd order low-pass TIA stage**

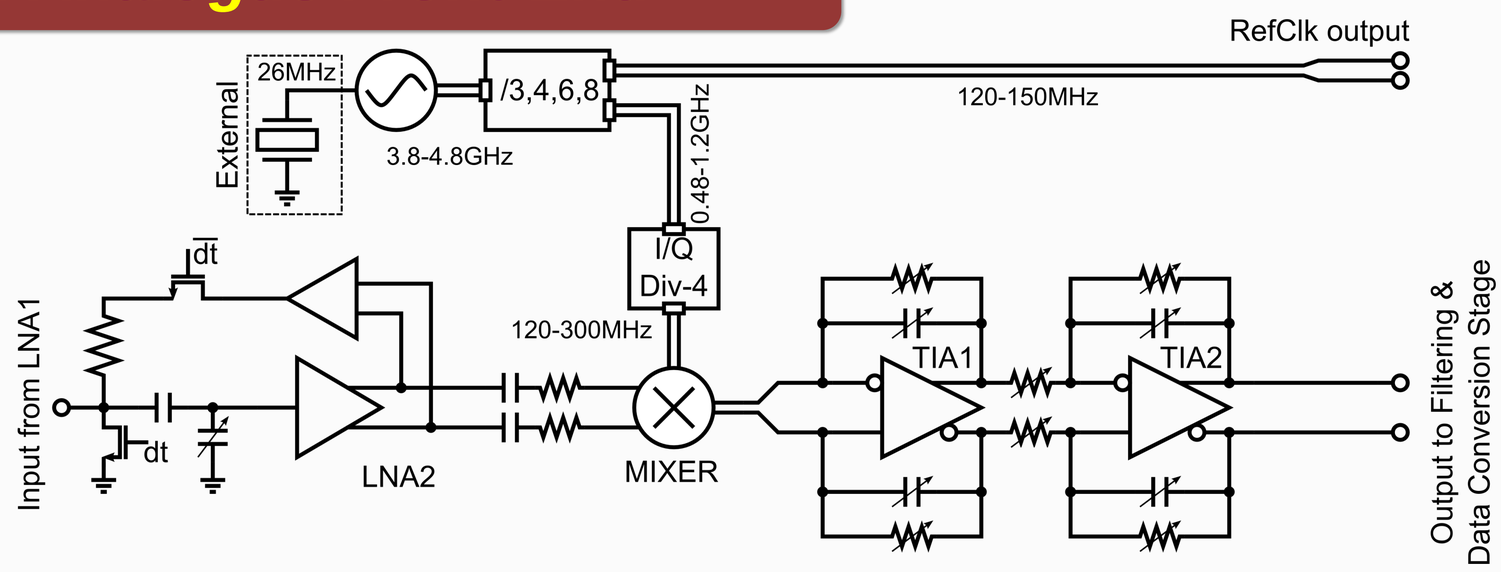

Fig. 3: Schematic of the analogue MRI front-end.

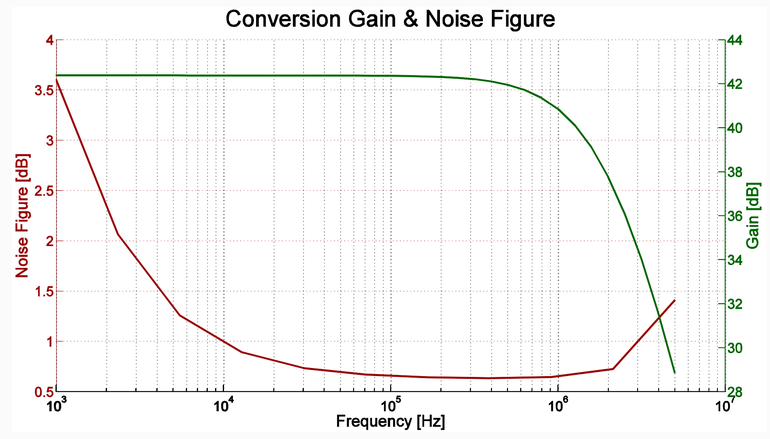

Fig. 4: Simulated gain and noise performance of the front-end.

4. Data Conversion & Filtering

- ❑ **Low-pass SD modulator in 130nm CMOS (BW=10MHz, DR=89dB)**
- ❑ **6th order Chebyshev filter in 130nm CMOS**

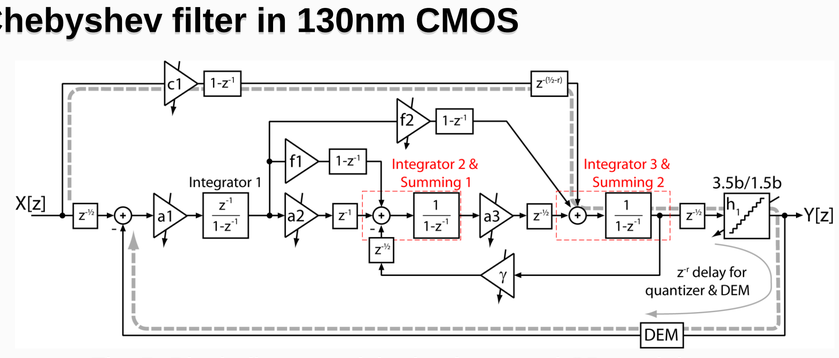

Fig. 5: Block diagram of the implemented SD modulator.

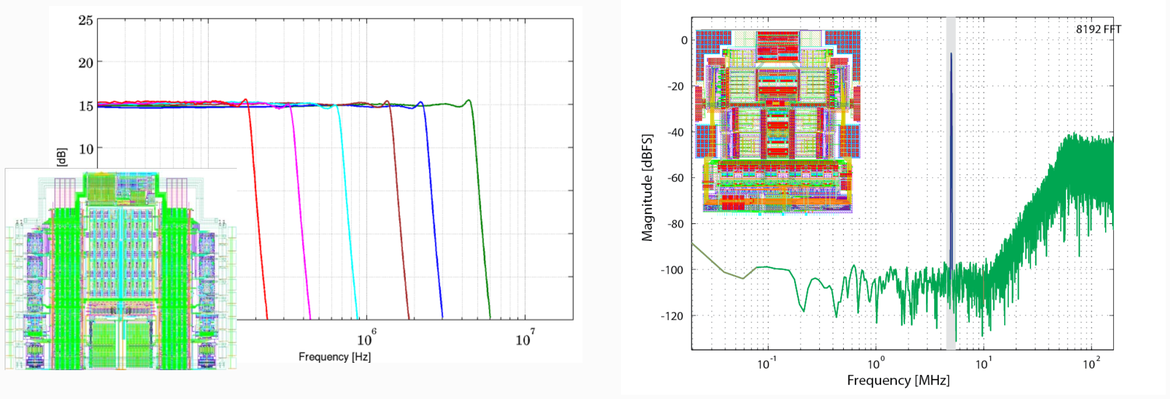

Fig. 6: BB filter transfer function for different modes (left), and simulated output spectrum for a 5MHz sinusoidal input signal (right). Corresponding layouts are shown in the insets.

5. Performance Summary

	Front-End	ADC	Total
NF	0.7dB	0.8dB	1.4dB
Gain	12…42dB	0dB	12…42dB
IIP3	-2dBm	2.5dBm	-3dBm
Power	80mW	20mW	~150mW
Area	1.1mm^2	0.3mm^2	~5mm^2

Fig. 7: Simulated performance summary (NF/IIP3 measures referred to the input coil)

References:

[1] B. Dietrich, et al. “A stand-alone system for concurrent gradient and RF sequence monitoring,” ISMRM 2012: 700.

[2] N. De Zanche, et al. "Modular design of receiver coil arrays," NMR in Biomedicine 21.6 (2008): 644-654.

[3] J. Rogin, et al. "A 1.5-V 45-mW direct-conversion WCDMA receiver IC in 0.13-µm CMOS," Solid-State Circuits, IEEE J. Solid-State Circuits, vol. 4, no. 12, pp. 2239-2248, Dec. 2003.