

# An Ultra-Low Power Asynchronous Data Interface

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**ETH**

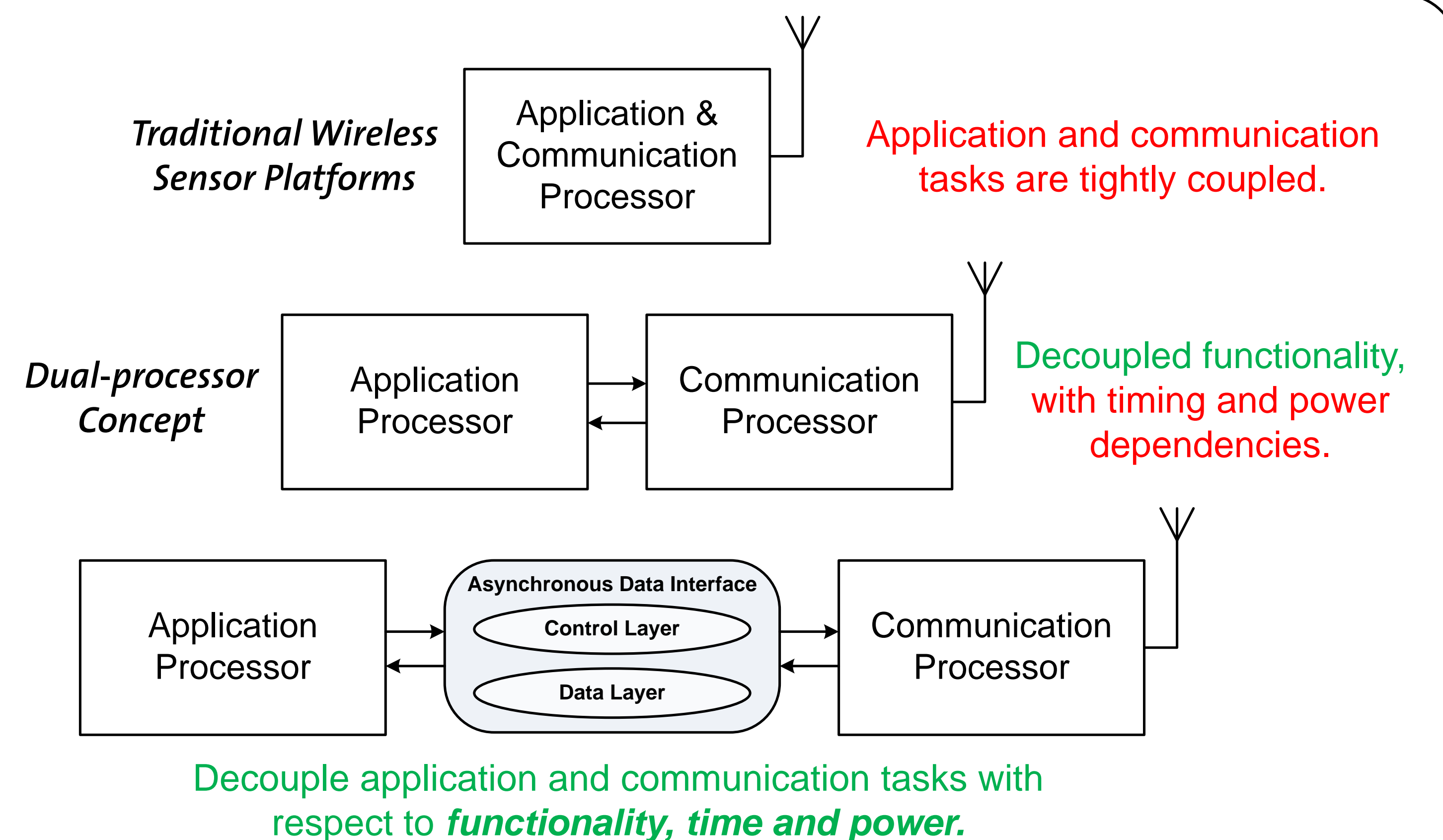
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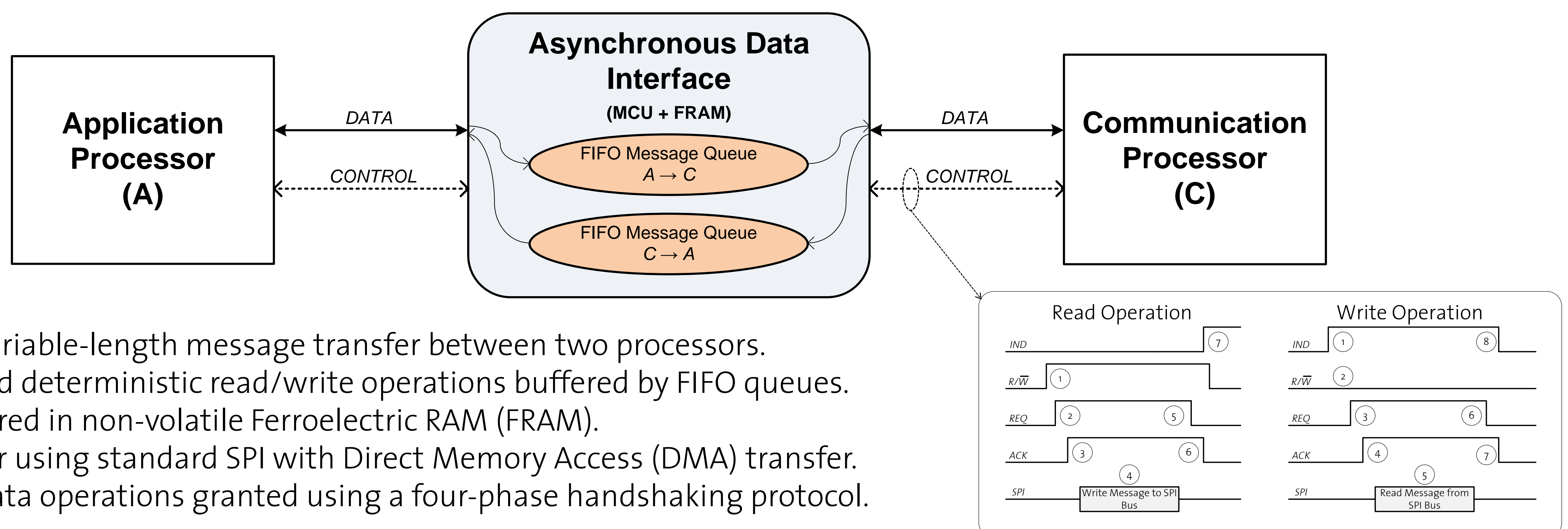
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## > Motivation

- Traditional wireless sensor platforms combine application and communication tasks on a single processor.
- However, application (e.g. event-driven sensing) and communication (e.g. synchronous protocols) tasks can not be preempted due to their strict timing constraints.
- This leads to contention on the single-processor platform, which severely impacts the application and/or communication tasks.
- Offline/online task scheduling is infeasible due to the unknown dynamics of the network and the physical process being sensed.
- Need a dual-processor architecture where application and communication tasks are decoupled in functionality, time and power.



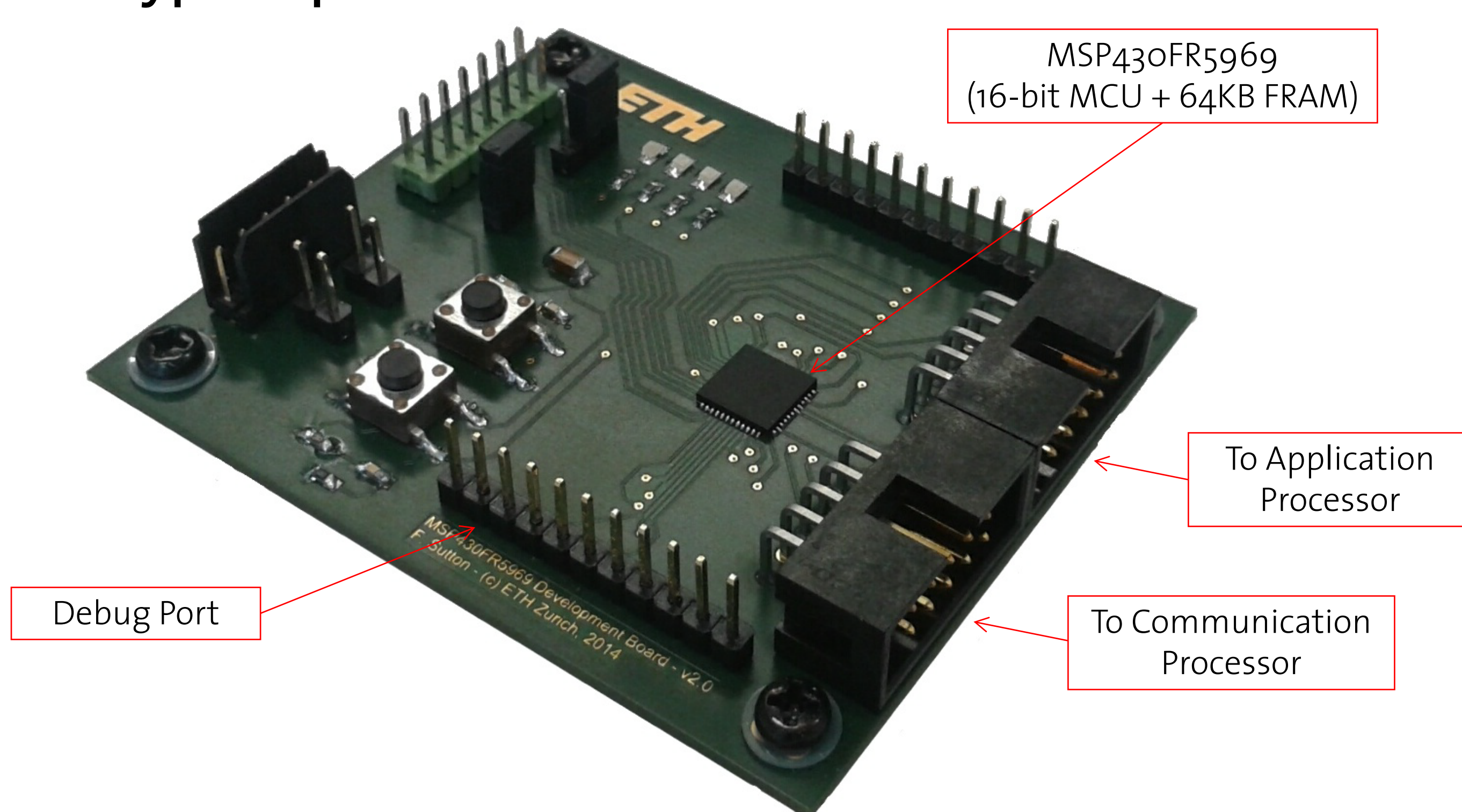
## > Interface Architecture



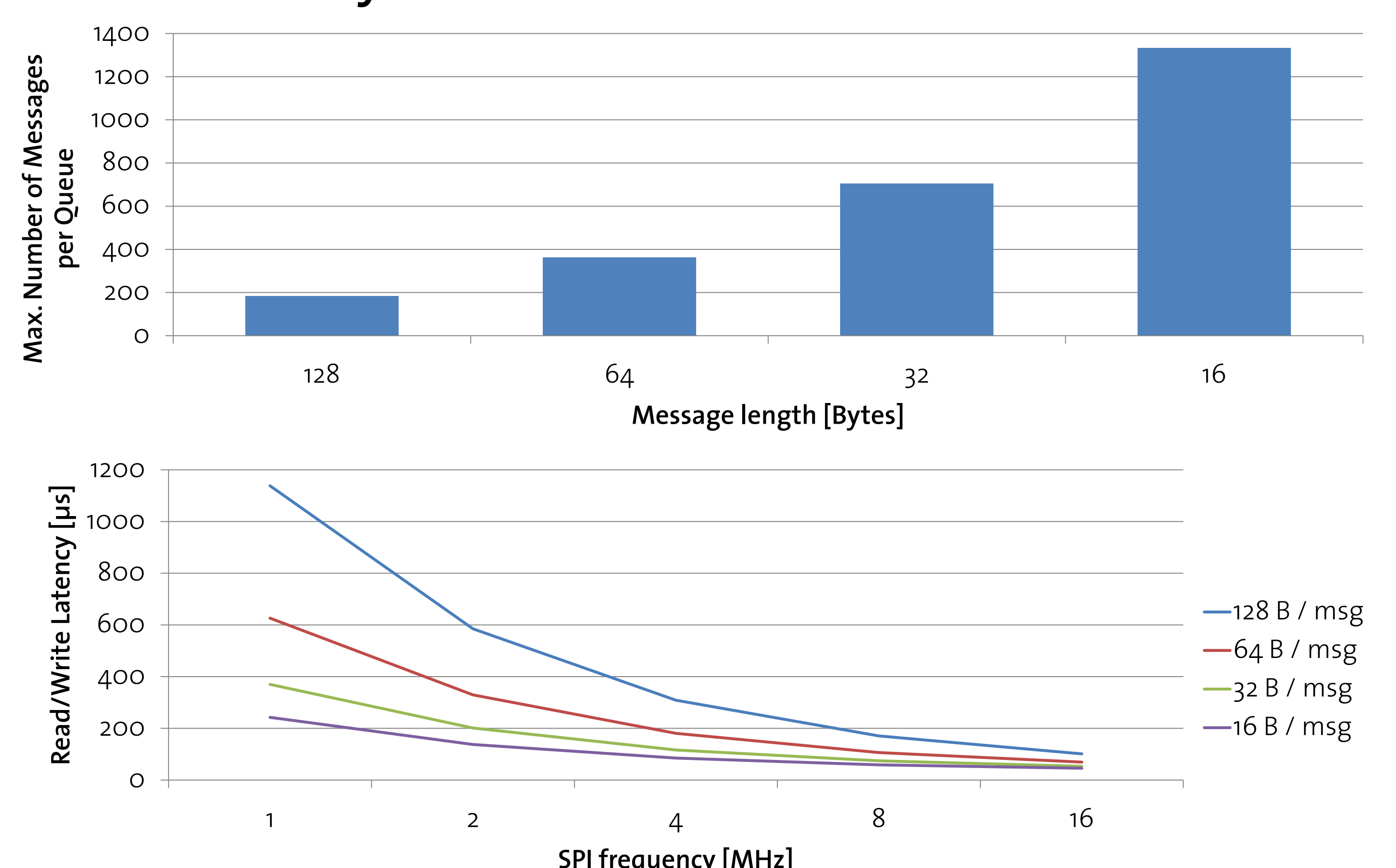
- Asynchronous variable-length message transfer between two processors.
- Non-blocking and deterministic read/write operations buffered by FIFO queues.
- All messages stored in non-volatile Ferroelectric RAM (FRAM).
- Message transfer using standard SPI with Direct Memory Access (DMA) transfer.
- Asynchronous data operations granted using a four-phase handshaking protocol.

## > Prototype Evaluation

### Prototype Implementation:



### Performance Analysis:



- State-of-the-art ultra-low power MSP430 with integrated FRAM.
- Interrupt driven implementation incorporating power optimizations.
- Idle power dissipation: **1.44µW @ 3.0V**
- Read/write operation latency: **< 200µs for 8MHz SPI bus**  
**< 300µs for 4MHz SPI bus**  
**< 1.2ms for 1MHz SPI bus**

Mode	Interrupt Handling (ACTIVE)	Read/Write Operation (LPM1)	No Operation (LPM4)
Current @ 1 MHz [µA]	128	47	0.48
Current @ 8 MHz [µA]	470	112	
Current @ 16 MHz [µA]	855	174	
Wake-up delay [µs]	-	5.75	6