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Fast and Scalable System Simulation Of Many-Core Heterogeneous SoCs

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ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

Motivation and Challenge

Demand for Hardware Acceleration
(On Chip Many-Core Accelerators)

Xeon Phi Coprocessor

Hybrid Cores
AMD Fusion (on-chip)

STHorm
STmicroelectronics
Heterogeneous
IOw poweR Many-Core

Epiphany Multicore Coprocessors

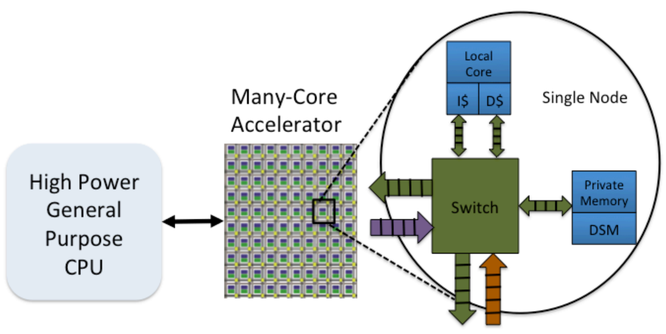
Tile based Manycores
Intel SCC, Tile 64
(Integrated)

Architectural Simulation of Heterogeneous SoCs

Current simulation methods are sequential and slow

Need for a fast, parallel, scalable and inexpensive solution for simulation

Solution – GPGPU Acceleration



Target Architecture

- Data-Parallel Coprocessors
- Simple In-order Cores
- RISC ARM and CISC x86
- 1000s of cores in a tile network
- Fine grain parallelism

Target Architecture **Host Platform**

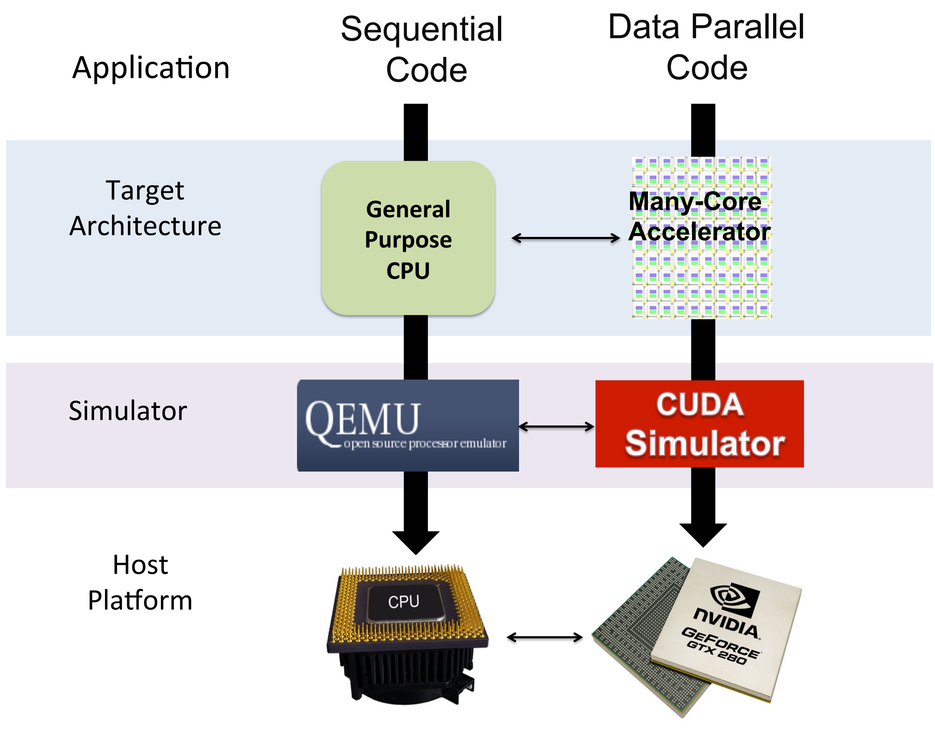
A Perfect Match

Simulation Features

- Instruction Accurate
- Inexpensive and Easily Available
- Fast Development Cycle
- Portability (Target Independent)
- Interpretation based core-simulation

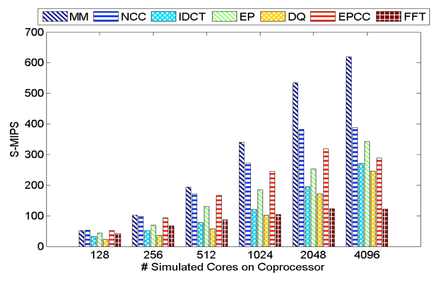
Simulation Framework

Parallel Target → Parallel Simulator → Parallel Host



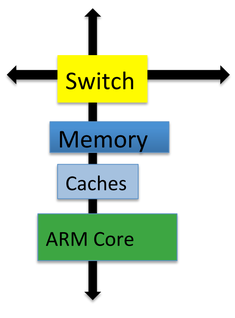
Experimental Results

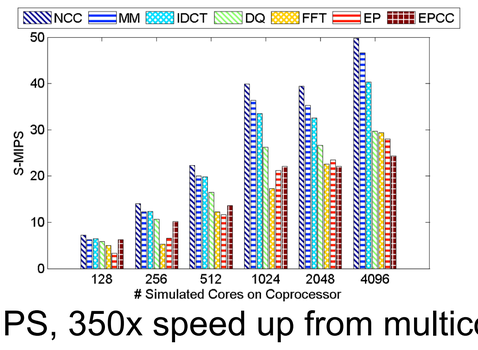
ARM ISA ↔ Data Scratchpad, Inst Scratchpad



600 MIPS, 800x speed up from multicore host

Single tile of target Accelerator

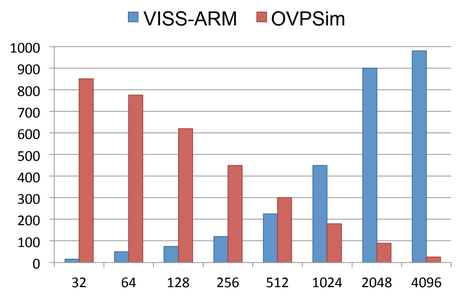




50 MIPS, 350x speed up from multicore host

Comparison with OVPSim

OVPSim – State-of-the-art parallel simulator on Multi-core Host



Better simulation performance with increasing number of cores

~800x speed up

Breakeven at simulation of 512 cores

Conclusion

- Challenge - and parallel simulator for heterogeneous SoCs
- Solution - Parallelize 1000 core simulation using GPUs
- Design - Full System Simulation using QEMU and SIMinG-1k
- Results - High Scalability and speedup upto 4096 cores