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BodyPoweredSenSE RTD 2013

FNSNF

Design of Integrated Power Converter for Ultra-Low Power Body Energy Harvesters

Milad Ataei, Christian Robert, Alexis Boegli, Pierre-André Farine

EPFL, IMT, ESPLAB, Neuchâtel, Switzerland

http://bodypoweredsense.ch/

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Introduction and Motivation

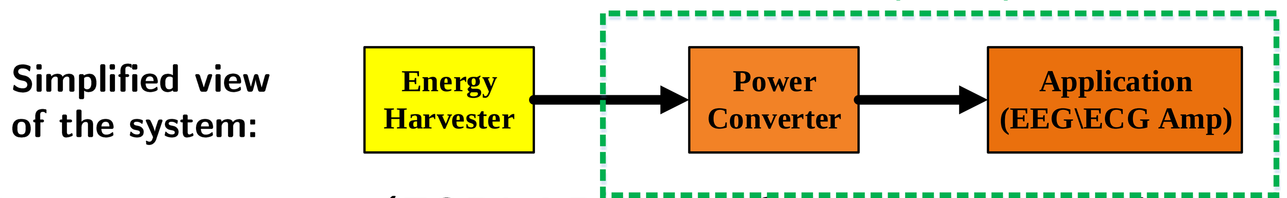
- Alzheimer's disease affects approximately 40 million people world wide
- 1 in 200 children of secondary school age suffer epilepsy
- EEG study for epilepsy can take up to a week.

BodyPoweredSenSE Project:

- The project will develop smart, energy aware, user friendly wearable sensors and associated medical algorithms for the early diagnosis of Alzheimer's disease and childhood epilepsy
- Since batteries have drawbacks including size, weight, operating lifetime or convenience in a wearable sensor, the goal is developing Advance "fit and forget" HEHMP (Human Energy Harvesting Medical Platform).

Issues in Human body energy harvesting:

- Body energy harvesters produce unreliably small power at low voltages.
- Power converter is then responsible for tapping such low potential energy and provide it as a high potential and reliable power source for applications.



Power converter (ESPLAB part) for body energy harvesting challenges:

- Extreme low power generators ➞ Optimize power converter efficiency
- Have to fit in an EEG electrode ➞ Integrated circuit & limited passive sizes

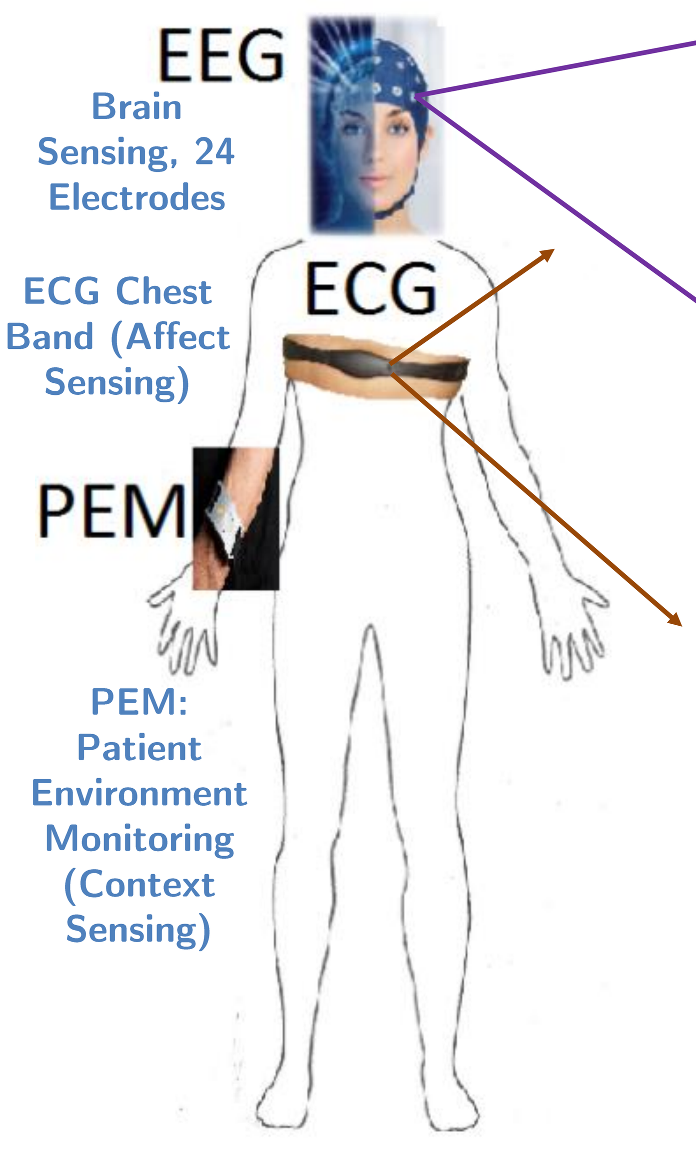
Previously existing solutions:

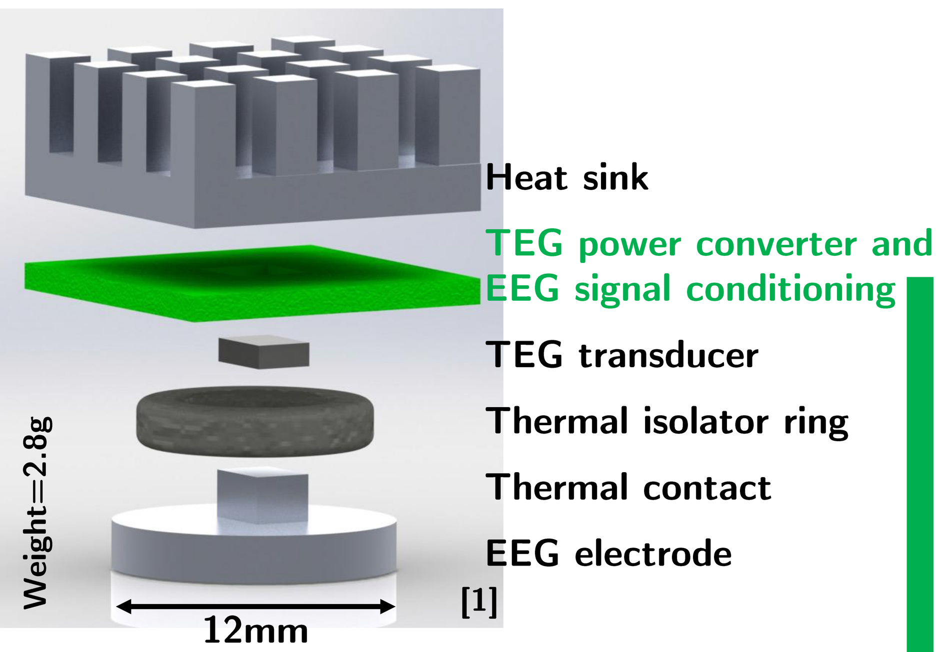
- Low voltage converters have already been achieved but not with ample efficiencies at extreme low voltage.
- Small form factor has not been considered for a such converter

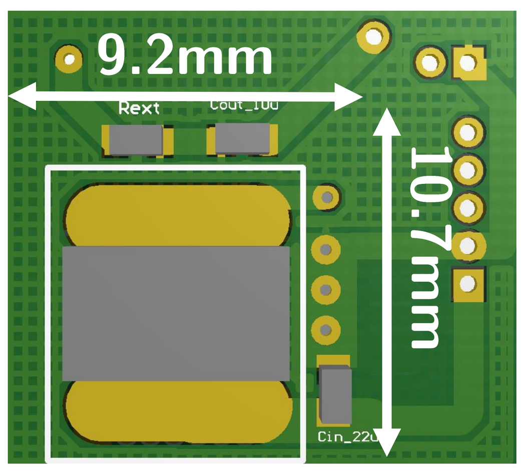
System implementation

The light weight EEG signal monitoring devices must maintain an acceptable precision. This becomes possible if active amplifier and signal conditioning are placed right next to the electrodes. Active components need an energy budget and batteries have the mentioned concerns, therefore, an autonomous active EEG electrode which consist of an EEG electrode, Thermo-Electric Generator (TEG) harvester, TEG power converter and amplifier is the proposed solution.

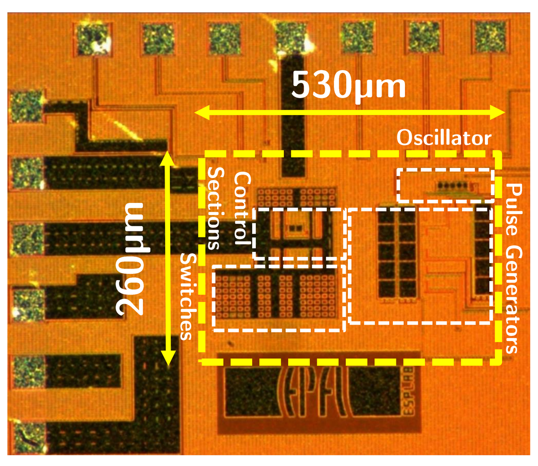
EEG/ ECG Active Electrode

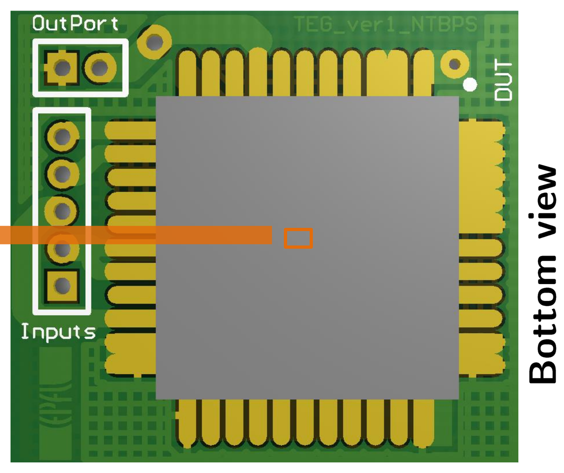




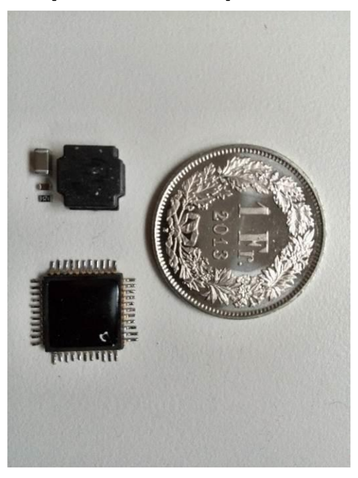


Designed PCB with a small form factor





Required Components



Design procedure

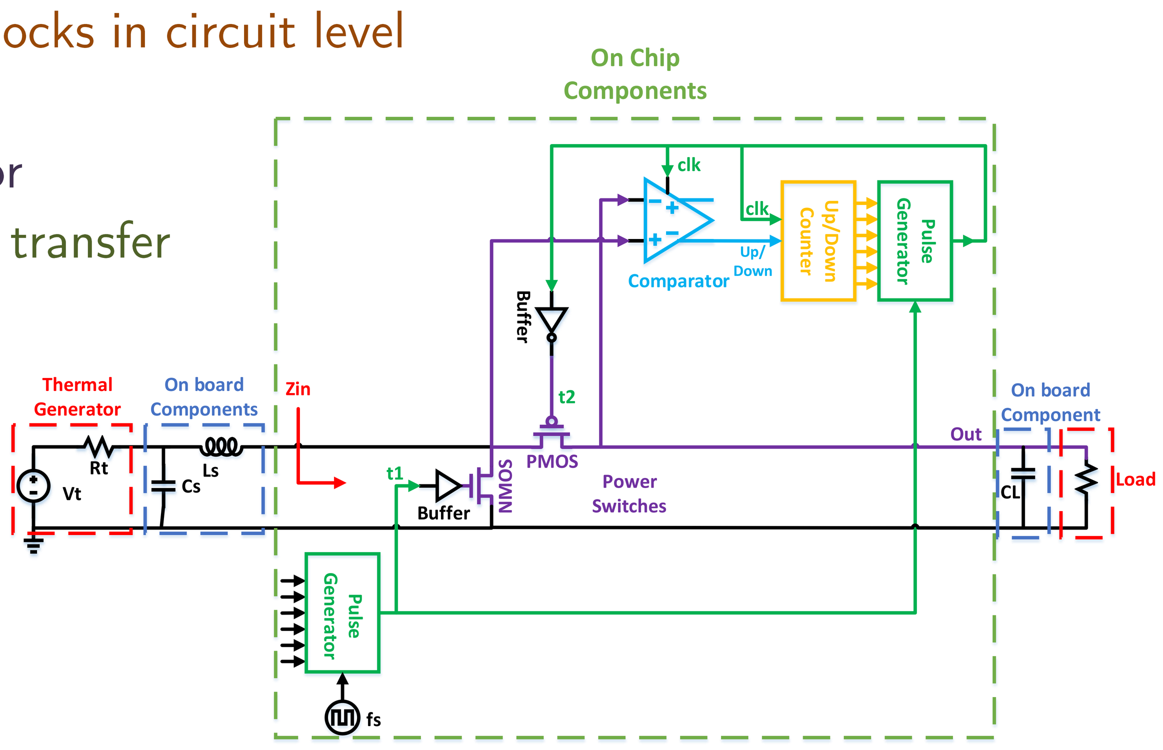
To realize a high efficient system here, 4 criteria have to keep in mind:

C1- Ultra low power blocks in circuit level

C2- Minimizing loss

C3- Limited form factor

C4- Maximizing power transfer



Fulfilling C1:

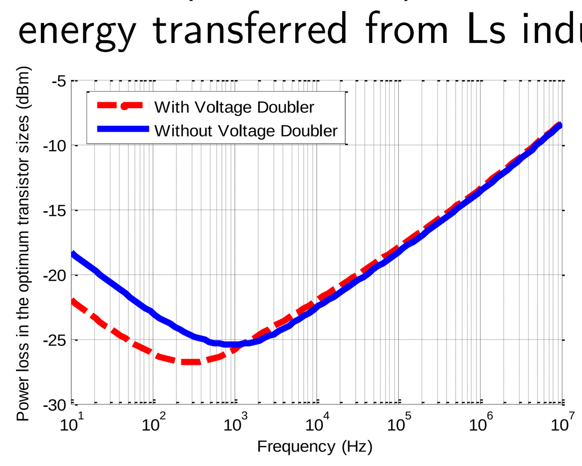
Considering the relative low switching frequencies involved (<10kHz), circuit blocks including comparator and control sections are dynamically powered, resulting in a minimized the power consumption

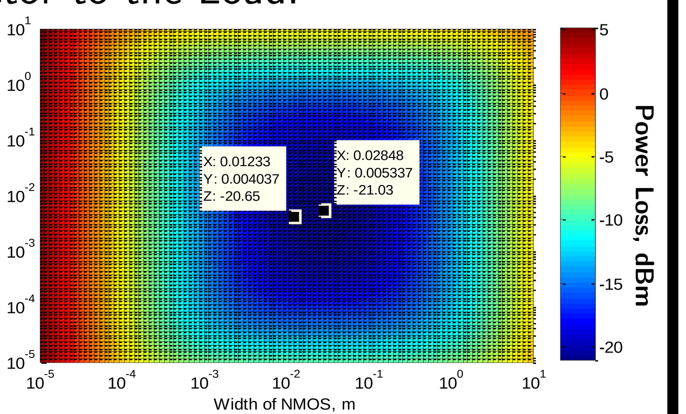
Phase 1 (t1 duration)- NMOS "on", PMOS "off" => energy stored in inductor Ls

Phase 2 (t2 duration)- NMOS "off" and PMOS "on" => energy transferred from Ls inductor to the Load.

Fulfilling C2:

In loss mechanism, there is a trade-off in the switches sizing and working frequency. Since static power losses changes in opposite of dynamic power loss, solving the losses' equations permits to find optimums.

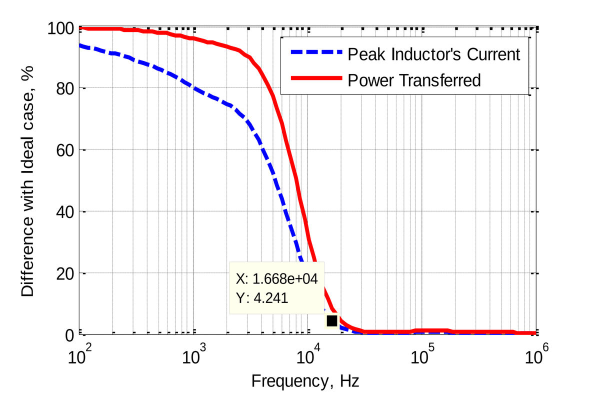


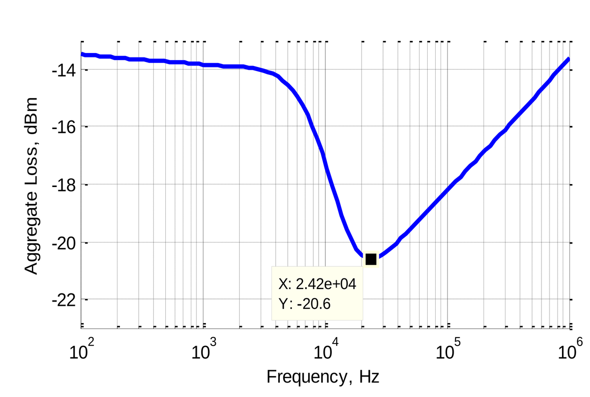


$$W_{n,opt} = I_{Ls,RMS,t1}\sqrt{\frac{R_{NMOS,0}}{f_s.\beta.C_{N,0}}}$$

$$W_{p,opt} = I_{Ls,RMS,t1}\sqrt{\frac{t_2}{t_1}\cdot\frac{R_{PMOS,0}}{f_s.\beta.C_{P,0}}}$$

$$\beta = V_{SW}^{2}\eta_{SW}\left(1+\frac{1}{\alpha}\right)$$





Fulfilling C3 and C4: Considering the limited size, the largest fitting inductor was selected and the chip have been designed in accordance to its value. Deviation of power transferred from ideal was then calculated and the final optimum frequency is derived based on that and losses.

Measurement results and conclusion

The equations for energy transfer and losses were used to design a general power converter and to reach efficiency limits of the architecture. All the parameters were calculated so that the final electronic board can be mounted in an active EEG electrode.

	Carlson, *JSSC* 2010	Bandyopadhyay, *JSSC* 2012	Shrivastava, *JSSC* 2015	This work measurement
Topology	Inductor based	Inductor based	Inductor based	Inductor based
Technology	0.13μm	0.35μm	0.13μm	0.18μm
Voltage Conversion	20mV~100 mV =>1V	100mV => 2V	20mV~300 mV => 1V	10mV~400m V => 0.9V
Output Power	25μW @20mV	1.3mW @100mV	-	22μW @20mV
Quiescent Power	1.3μW	-	0.3μW	1.6μW
η at 20mV	46%	40%	21%	54%
η at 100mV	68%	65%	68%	71%
Core area	0.12mm²	2.5mm²	0.12mm²	0.14mm²

3 different type of TEG are considered in this project. The system have to, at least, supply the integrated EEG amplifier.

	O.C. Output Voltage of TEG	TEG output Impedance	TEG Available Power	Power needed for amplifier	Measured Output Power of system	Efficiency of system	Usability for the project
Thermal 1	20-40mV	2.5Ω	40-160μW	5μW	22-128μW	54%	OK
Thermal 2	80-200mV	182Ω	8.8-54μW	5μW	5.3-44μW	60-80%	OK
Thermal 3	100-400mV	50Ω	50-800μW	5μW	35-458μW	58-70%	OK

References:

[1] M. Thielen, M. Ataei, et al. , *International Conference on Thermoelectrics - ICT2014*, 2014

[2] M. Ataei, et al., *In Journal of Physics: Conference Series, vol. 557, no. 1, p. 012017. IOP Publishing*, 2014

[3] M. Ataei, et al. , *Journal of Micromechanics and Microengineering* (under full peer-review), 2015

Electronics and Signal Processing Laboratory

esplab.epfl.ch

Contact: milad.ataei@epfl.ch