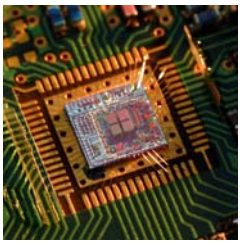
nano-tera.ch
swiss scientific initiative in health / security / environment systems

icySoC RTD 2013

FNSNF



Sub- and near-threshold standard cell design for low-power applications

csem

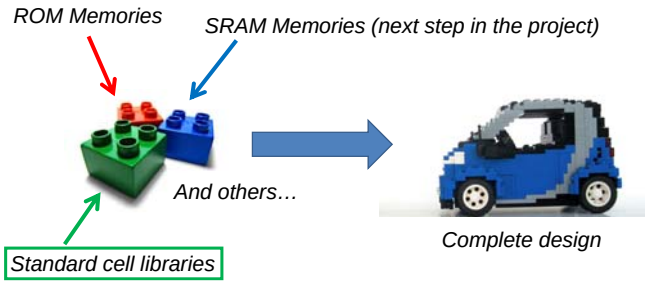
Marc Pons[1], Daniel Séverac[1], Christian Piguet[1], Philippe Rochaix[2], Thomas Lentsch[2]

[1] CSEM Centre Suisse d'Électronique et de Microtechnique SA, [2] EM Microelectronic-Marin SA

The main goal of sub- or near-threshold design (i.e. integrated circuits supplied with a voltage lower or just above MOS transistor threshold voltage) is to reduce the dynamic power consumption by decreasing the supply voltage. Working at lower voltages than regular circuits opens the door to better power efficiency. However, at these low voltages, digital standard cell libraries need to be revisited to ensure the correct operation of integrated circuits. To fulfil the requirements of the specific application, libraries can also be optimized for constraints like frequency or static power consumption. This motivates the comprehensive study of trade-offs in the design of sub- and near-threshold standard cell libraries. A first library for the EM Microelectronic Marin ALP 180 nm technology has been developed focusing on ultra-low-power optimization by limiting the leakage power within given frequency requirements. A second library for TSMC 65 nm has been developed to reach the minimum supply voltage level for applications with energy harvesting. Both libraries will be used as building blocks for the circuit integrations planned in the icySoC project in order to demonstrate the capabilities of sub- and near-threshold design.

Building blocks for low-power circuits

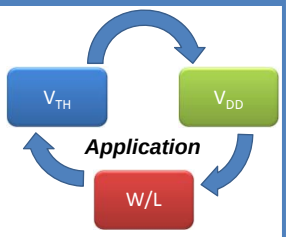
- Early specification and careful selection and development of the building blocks of low-power circuits (e.g. standard cell libraries) ensure successful design for a given application (i.e. dynamic power, static power and frequency requirements)



Sub- & near- threshold standard cell choices

V_{TH} selection

- low-V_{TH} → lower minimum V_{DD}
- high-V_{TH} → lower leakage



Minimum V_{DD} selection

- low-V_{DD} → enables energy harvesting
- high-V_{DD} → lower upsize of W and L for robust operation

W/L selection

- Inverse Narrow Width Effect → W upsize causes V_{TH} increase
- Reverse Short Channel Effect → L upsize causes V_{TH} decrease

V_{TH} = transistor threshold voltage; V_{DD} = supply voltage; W/L = transistor width and length

ALP 180 nm standard cell library

Libraries considered

- SUB_LIB_SVT: standard-V_{TH} library sized for 0.6 V min.
- SUB_LIB_LVT: low-V_{TH} library sized for 0.4 V min.
- LIB_SVT: standard-V_{TH} library from the foundry at 0.9 V min.
- LIB_LVT: low-V_{TH} library from the foundry at 0.72 V min.

Test vehicle circuit evaluation

- Test vehicle: digital circuit using latch-based design with a critical path depth of 45 cells and an equivalent gate count of 10'000 gates

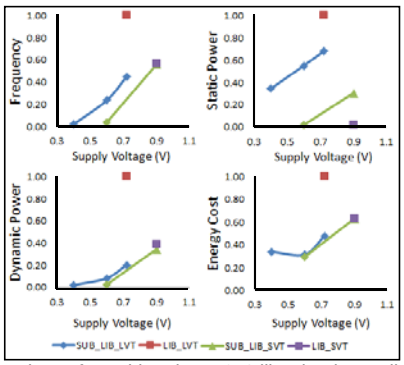


Figure I: Comparison of considered ALP 018 libraries (normalized values)

ALP 180 nm library selected

- SUB_LIB_SVT: standard-V_{TH}, V_{DD}=0.54 V min, L=300 nm, 72 cells
- Goal: Frequency at 0.9 V similar to LIB_LVT at 0.72 V and static power at 0.6 V comparable to LIB_SVT at 0.9 V
- Works in a wide range of power supplies

TSMC 65 nm standard cell library

Libraries considered

- SUB_LIB_LVT: low-V_{TH} library sized for 0.3 V min.
- LIB_HVT: high-V_{TH} library from the foundry operating at 1.0 V min. (classical low power library)

Test vehicle circuit evaluation

- Test vehicle: CSEM's **icyflex2** ultra-low-power processor in battery operated applications, such as portable medical and wireless sensors. It can also be used as an microcontroller core, in a larger SoC, e.g. for handling power management.

	LIB_HVT 1.0V	SUB_LIB_LVT 0.3V	SUB_LIB_LVT 0.5V
Frequency	1	2.00 E-4	3.90 E-2
Area	1	2.84	2.56
Power	1	2.06 E-5	1.15 E-2
Power/Frequency	1	1.03 E-1	2.94 E-1

Table I: Comparison of the TSMC 65 nm libraries for flip-flop based design

	LIB_HVT 1.0V	SUB_LIB_LVT 0.3V	SUB_LIB_LVT 0.5V
Frequency	1	1.80 E-4	3.80 E-2
Area	1.04	2.10	2.12
Power	4.60 E-1	6.40 E-6	4.40 E-3
Power/Frequency	4.60 E-1	3.55 E-2	1.16 E-1

Table II: Comparison of the TSMC 65 nm libraries for latch based design

Results in Tables I and II are normalized to the LIB_HVT flip-flop icyflex2 implementation.

TSMC 65 nm library selected

- SUB_LIB_LVT: low-Vth, V_{DD}=0.3 V min, L=100 nm, 50 cells
- Goal: min V_{DD} for enabling energy harvesting
- Works in a wide range of power supplies
- Interest of latch based design for sub- and near-threshold operation