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Circuits and Techniques for Dynamic Timing Monitoring in Microprocessors

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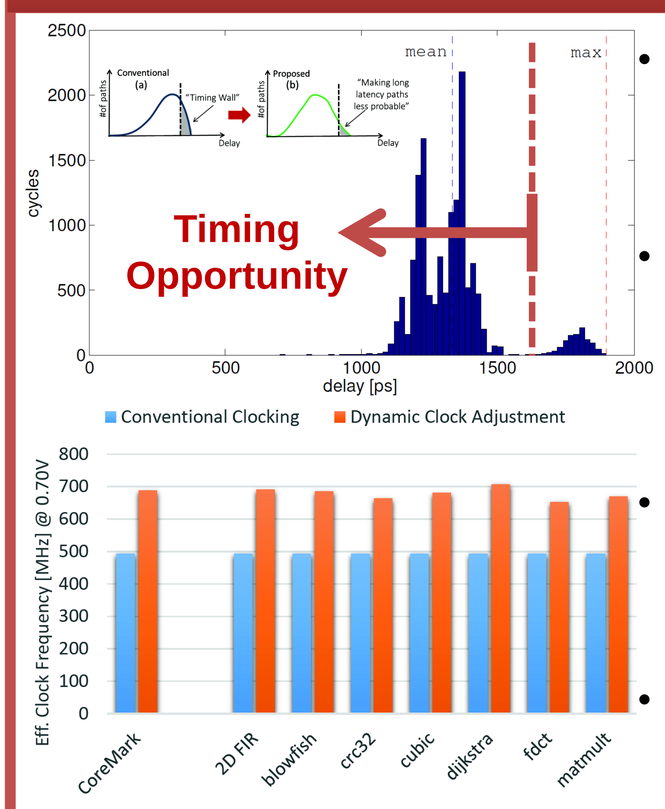
Abstract

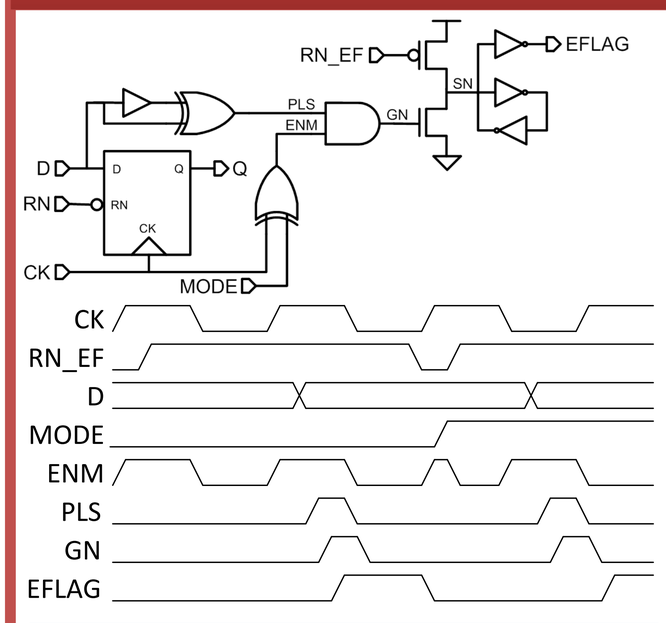
The maximum clock frequency at which a microprocessor core can be operated is typically based on the worst-case timing path estimated by the static timing analysis. However, depending on the design, this critical path is not always excited and therefore **dynamic timing margins** exist that can theoretically be exploited for the benefit of achieving higher speed or lower power consumption (through voltage scaling). A predictive dynamic **clock adjustment** technique is used to trim those timing margins by exploiting the different timing requirements of individual instructions in a processor [Costantin, DATE 2015]. In this scenario, the activation of each timing path must be continuously monitored by failure-detection mechanisms. A **timing monitor sequential (TMS)** is proposed with selectable error-detection window that allows for different techniques of timing investigation. The proposed circuit provides conventional error-monitoring, as usually performed by error-detection sequentials (EDSs), and it can be used for measuring the maximum clock frequency required by each processor instruction as well as for predicting timing errors. These techniques will be used in the future to detect timing errors in DSP circuits to exploit dynamic timing margins by using approximations.

Exploiting Dynamic Timing in Processors



- **Critical path excitation** depends on the **current instruction** in each pipeline stage
- Measuring of maximum clock frequency for each instruction sequence with **predictive timing-error detection**
- Dynamic adjustment of the clock frequency based on the current state of the processor
- **Performance gain** of either +38% speed or -24% energy [Costantin, DATE 2015]

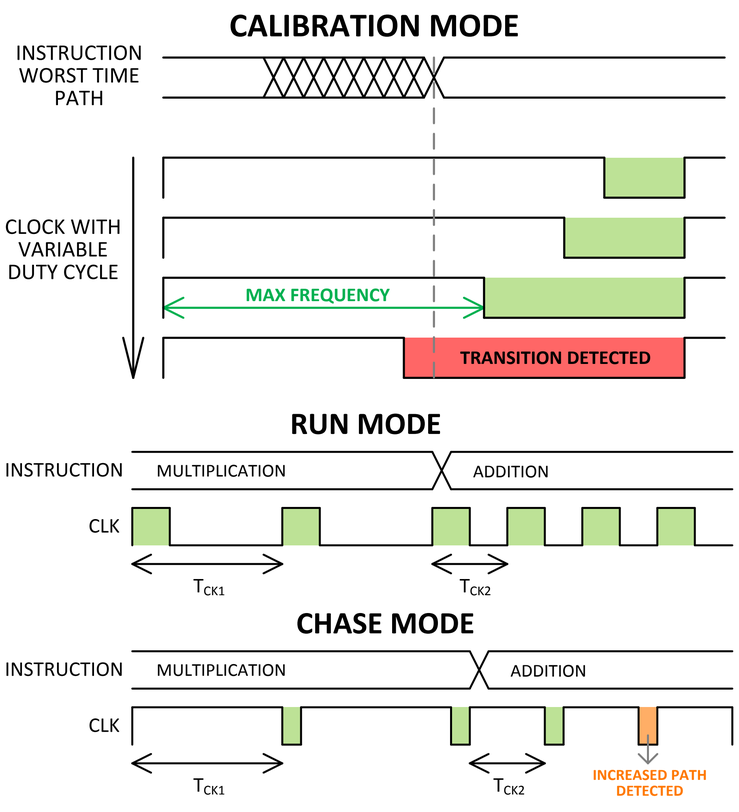
Proposed Timing Monitor Sequential



- **Forward Monitoring:** transitions detected on high phase of the clock
- **Backward Monitoring:** transitions detected on low phase of the clock

- Conventional EDS detects **late-arriving transitions** on the input
- Proposed TMS provides a **selectable error-detection window**
- Investigation and quantization of timing failure probability by the execution of different operation modes
- **Several applications:** Detection of timing errors due to VDD droops, noise, local variations, aging effects…

Operation Modes for Timing Investigation



- Timing of each instruction can be evaluated with TMSs and dynamic clocking
- **Calibration:** worst-time paths are measured in backward monitoring
- **Run:** each instruction is executed at the calibrated clock frequency
- **Chase:** add small timing margins to early detect timing-path degradation

Selectable error-detection window and dynamic clocking for:
- **Timing error prediction** with backward monitoring and additional timing margin on the clock period
- **Conventional error monitoring** for dynamic timing variations

Custom Design of the TMS

- Custom design reduces complexity and minimize parasitics
- The proposed TMS does not rely on pulse-generation as conventional EDSs for **improved robustness** at scaled VDD
- Monitoring of nodes that are **conditionally discharged**