IrSens2

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FPGA based control system for multi-component gas sensing

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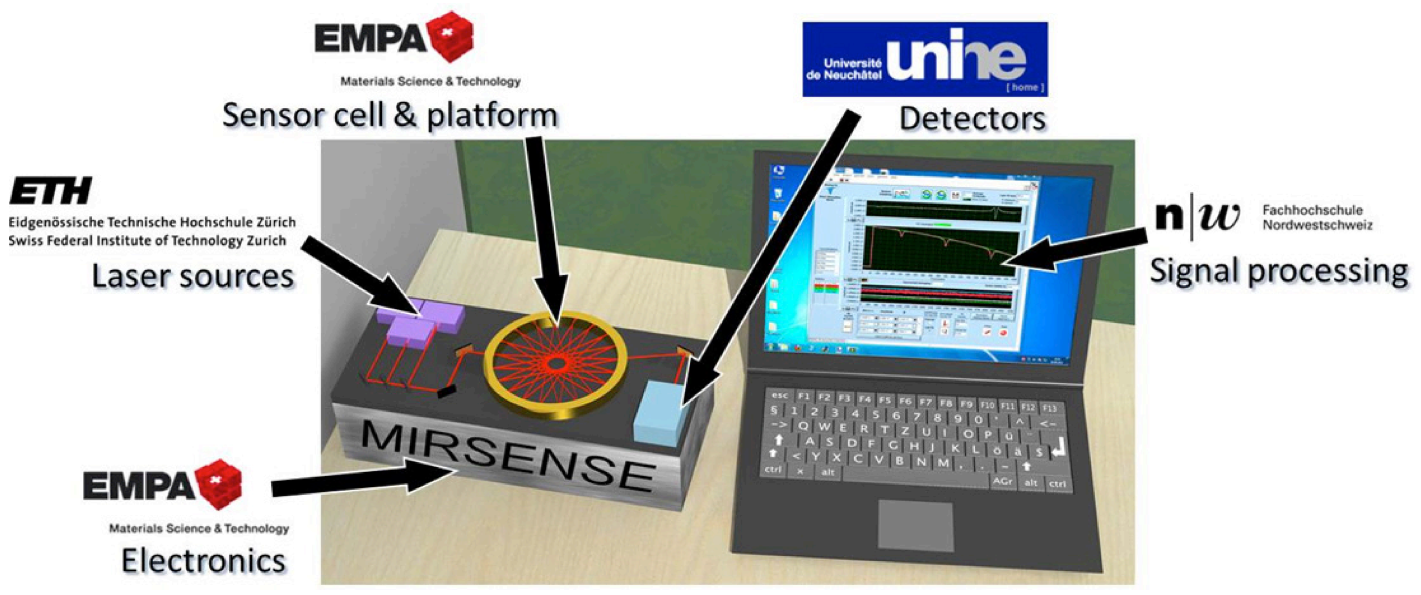
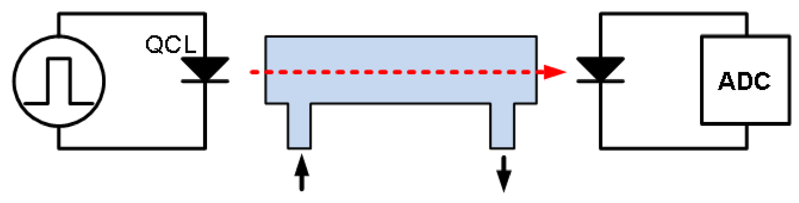
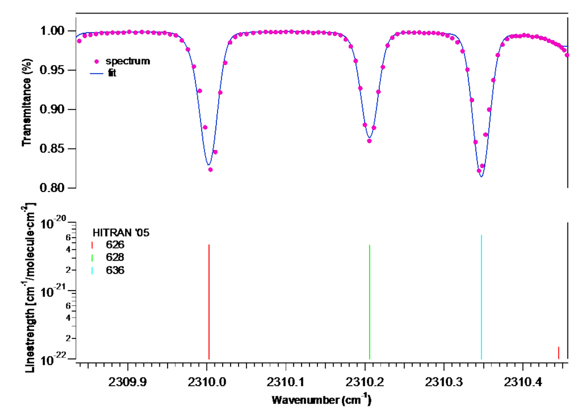
Introduction



In the project IrSens2 a **"multi-component sensor for air pollutants and greenhouse gases"** is being developed. A device using several quantum cascade lasers (QCL) in conjunction with a sophisticated absorption cell, low noise electronics, low power consumption and a small footprint results in a scientifically outstanding air monitoring system.

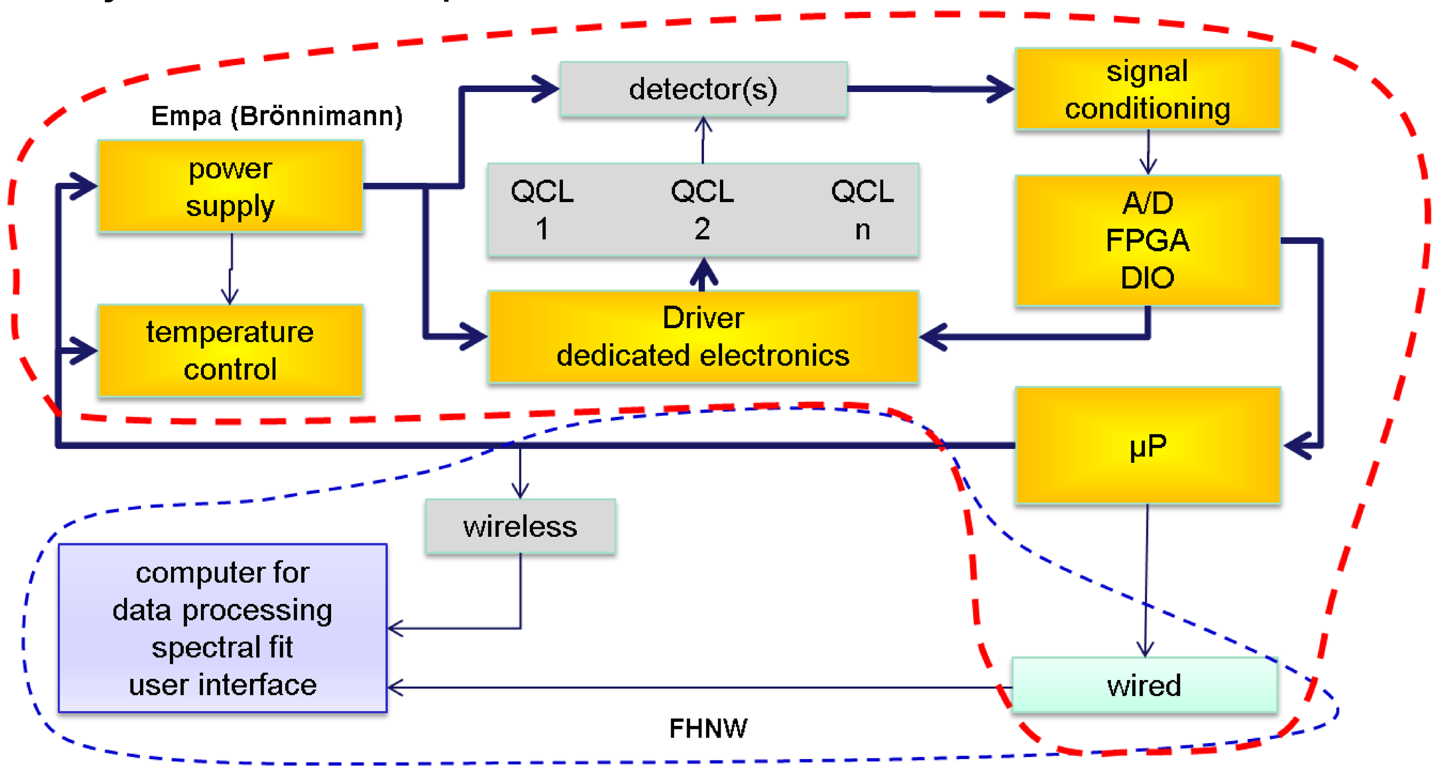


Principle of spectroscopy



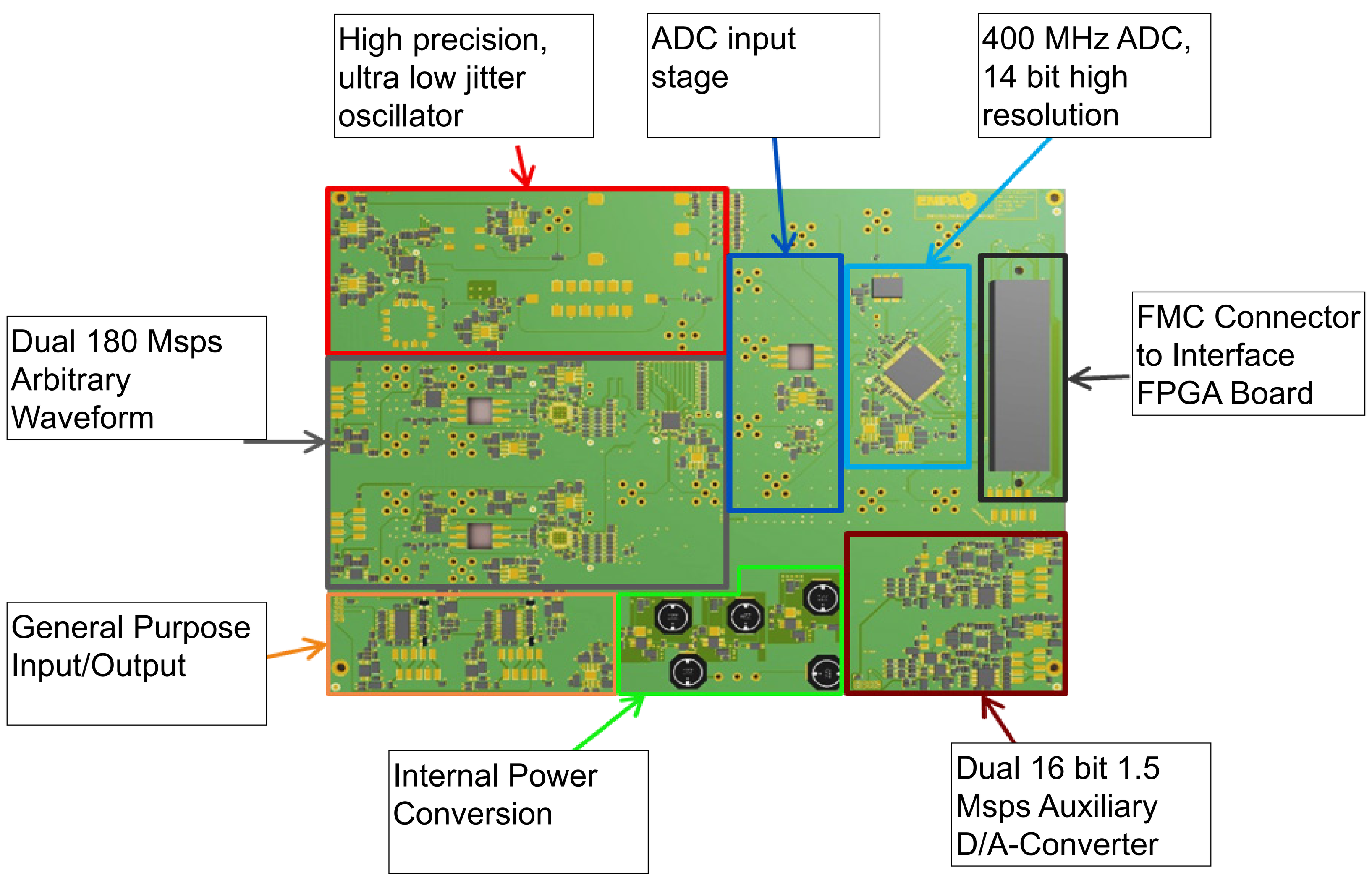
Control System

The requirements result in a complex control system. Laser driver, signal conditioning and digitalization are critical to achieve low noise. The complex timing, data acquisition and filtering is controlled by an FPGA in conjunction with a µP.



Hardware

A data acquisition board was realized comprising a high precision oscillator, 400 MHz high resolution ADC with input stages, fast analog outputs and a combined switched and linear power supply.



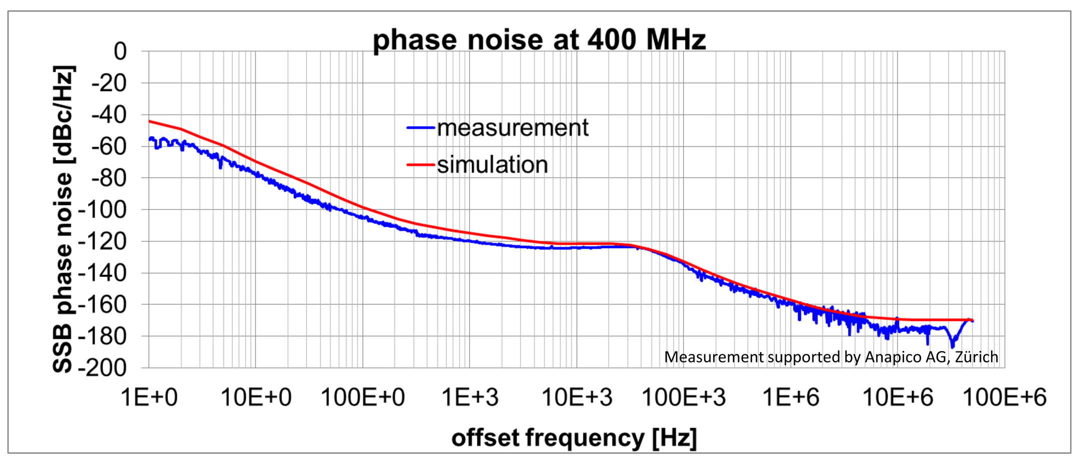
Results

Oscillator performance: Digitizing large high frequency signals requires a stable clock source. The measured phase noise of the developed oscillator is slightly lower than the simulation. The resulting phase jitter J in the range from 100 Hz to 50 MHz is below 100 fs.

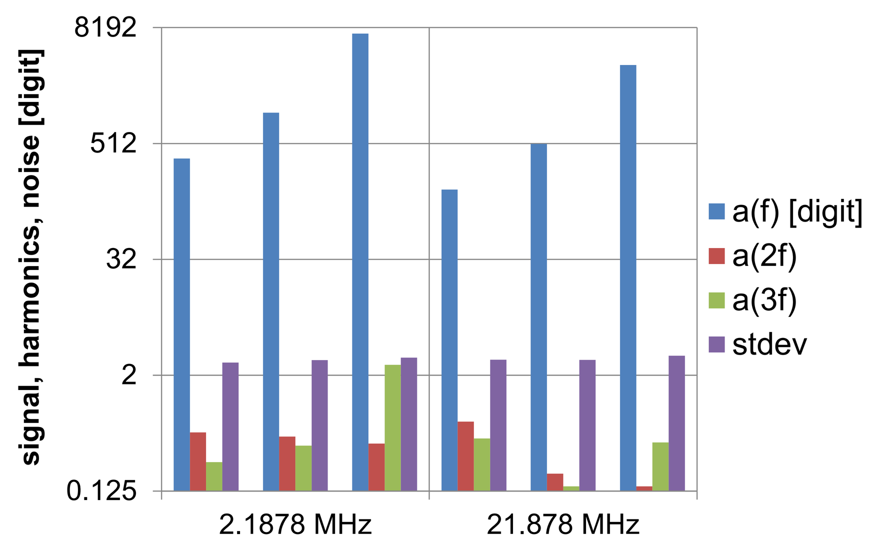
$$J = \frac{\Delta\phi}{2\pi f_c} = \frac{\sqrt{2\int_{f_1}^{f_2} \mathcal{L}(f)\, df}}{2\pi f_c}$$

$$J_{Tot} = \sqrt{J_{ADC}^2 + J_{CLK}^2}$$

Bandwidth	Simulation	Measurement
1 Hz – 50 MHz	2.43 ps	1.14 ps
100 Hz – 50 MHz	105 fs	**98.3 fs**

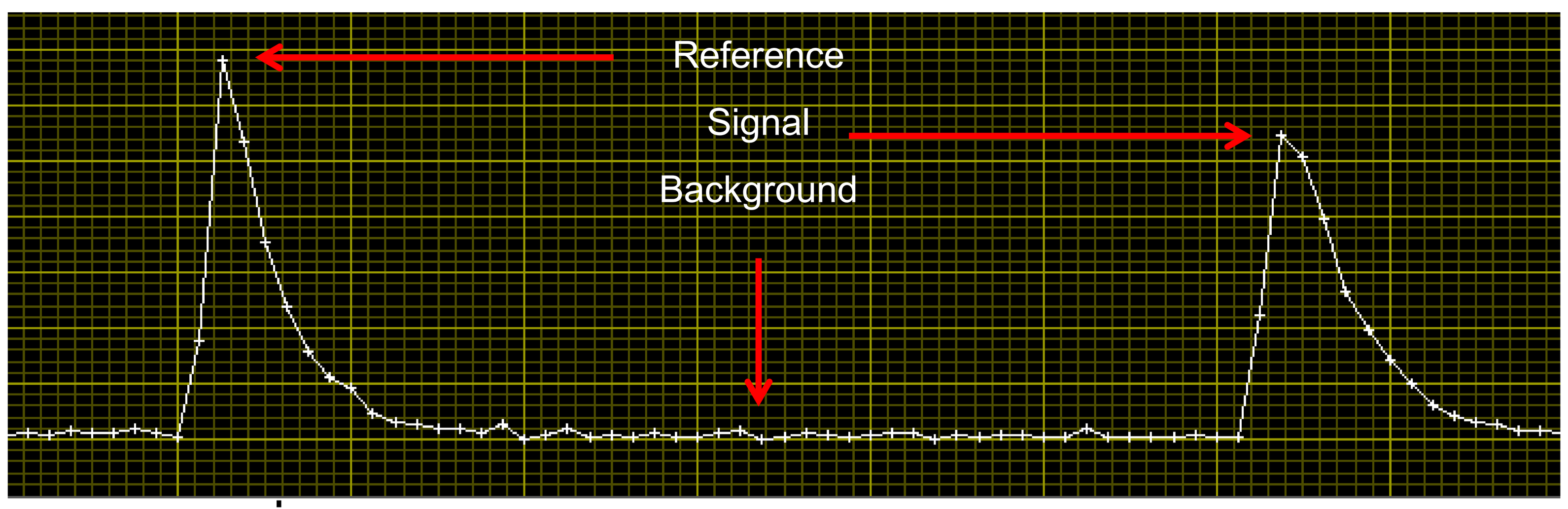


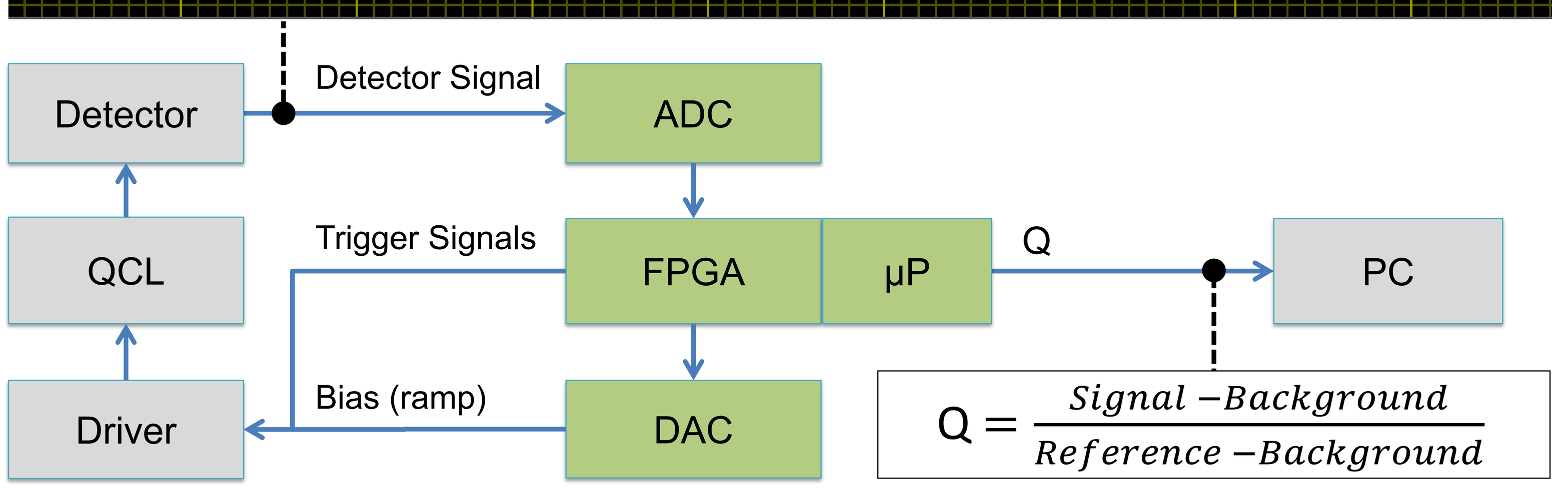
ADC performance:
- low harmonic distortion
- flat frequency response
- 3 digit noise level (full bandwidth) corresponding to 0.2 mV(rms)



Example of Data Evaluation

The wavelength of the pulsed QCL is tuned by a bias current.
Part of the laser pulse is directly fed to the detector resulting in a reference pulse, while the rest is guided through the multi-pass cell giving rise to a delayed signal pulse.
The FPGA extracts the peak heights and performs background compensation. The data can be pre-evaluated without information loss due to the high speed of the FPGA.
The data is then transferred to a PC where it is analyzed in detail.





References:

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