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Enhanced Interpolated-DFT for Synchrophasor Estimation in FPGAs: Theory, Implementation and Validation of a PMU Prototype

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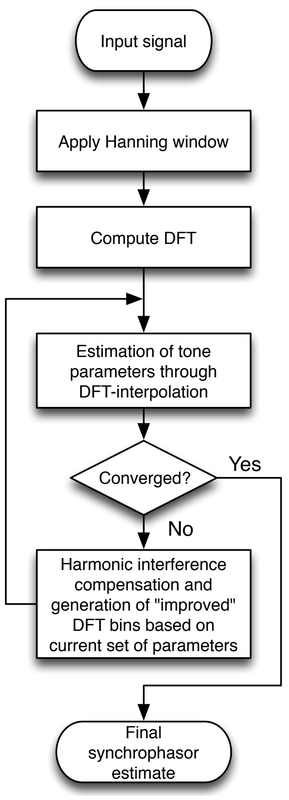
Aim of the research

The core component of any PMU is represented by the synchrophasor estimation algorithm, whose choice is driven by three main factors: (a) its accuracy, (b) its response time as well as (c) its computational complexity.
The literature on the subject of synchrophasor-estimation algorithms has already discussed the use of Interpolated Discrete Fourier Transform (IpDFT) as an approach capable to find an optimal tradeoff between synchrophasor estimation accuracy, response time and computational complexity. Within this category of algorithms this paper proposes two contributions: (i) the formulation of an enhanced IpDFT (e-IpDFT) algorithm that iteratively compensates the effects of the harmonic interference and (ii) the discussion of the deployment of IpDFT-based synchrophasor estimation algorithms into FPGAs, with particular reference to the compensation of the error introduced by the free-running clock of A/D converters with respect to the GPS time reference. The paper finally illustrates its compliance tests verification with respect to the accuracy limits defined in the IEEE Std. C37.118.1-2011.

e-IpDFT based Synchrophasor Estimation Algorithm

The algorithm presented belongs to the category of DFT-based synchrophasor estimation algorithms. It has been conceived to satisfy the following conflicting requirements: (a) good accuracy for both transmission and distribution networks applications; (b) feasible computational complexity enabling its implementation inside an FPGA.
The following correction approaches have been proposed for the correction of the typical error sources for DFT-based algorithms:

Considered error sources		Correction approaches
Aliasing	➔	Increasing of the sampling frequency (up to 50 kHz)
Long range spectral leakage	➔	(a) Windowing (b) Harmonic interference compensation
Short range spectral leakage	➔	DFT interpolation



$$s(n) = \overline{s} + \sum_{m=1}^{M} A_m \cos(2\pi f_m n\Delta t + \varphi_m)$$

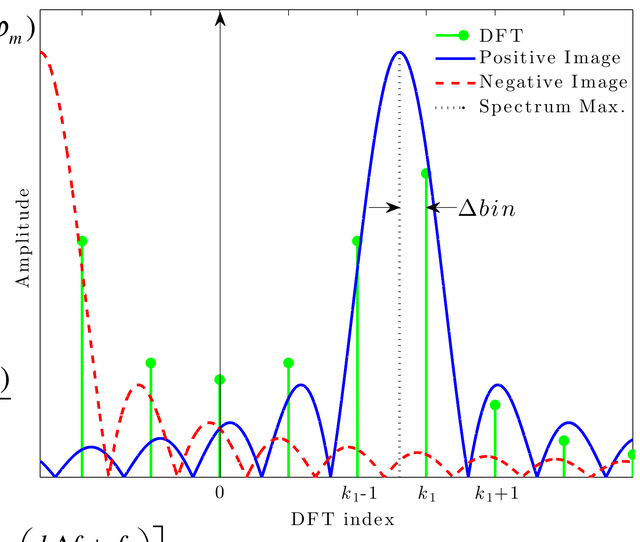
$$w(n) = 0.5\left[1 + \cos\left(\frac{2n}{N}\pi\right)\right]$$

$$S(k) = \frac{1}{B}\sum_{n=0}^{N-1} w(n)\cdot s(n)\cdot e^{-jk\beta_n}$$

$$\begin{cases} f_1 = & (k_1 + \Delta bin)\Delta f \\ A_1 = 2\left|S(k_1)\right| \cdot \dfrac{\pi\Delta bin\cdot(1-\pi\Delta bin^2)}{\sin(\pi\Delta bin)} \\ \varphi_1 = & \angle S(k_1) - \pi\Delta bin \end{cases}$$

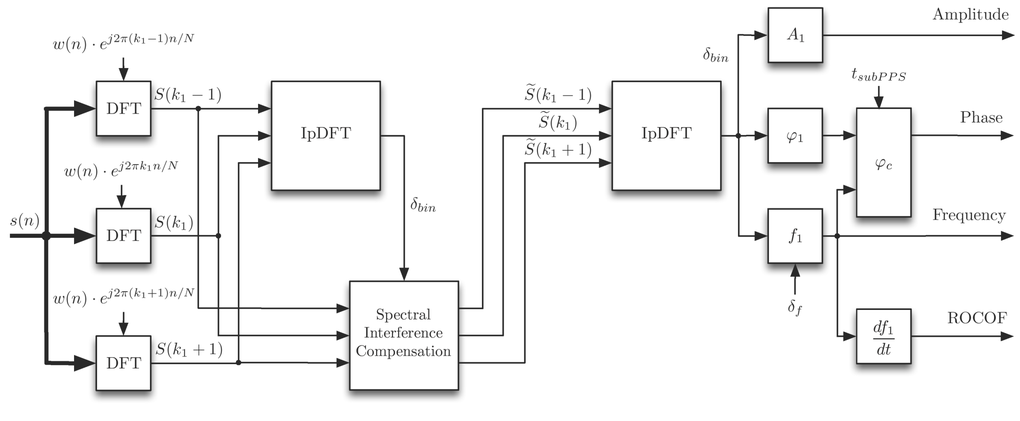
$$S(k) \approx \frac{1}{B}\left[V_1 \cdot W\left(\frac{k\Delta f - f_1}{\Delta f}\right) + V_1^* \cdot W\left(\frac{k\Delta f + f_1}{\Delta f}\right)\right]$$

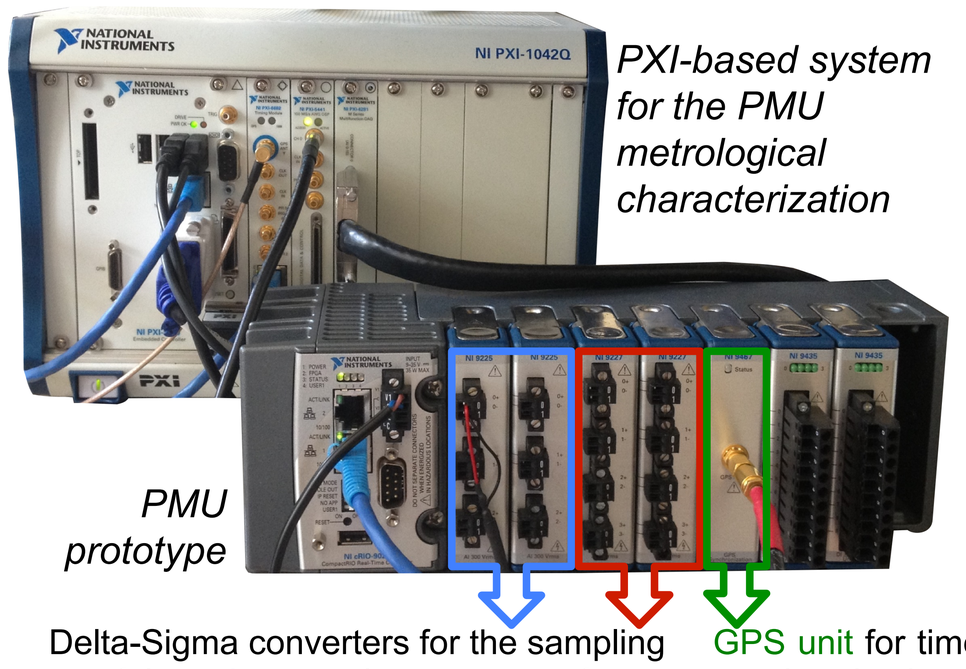
Positive Image Negative Image



Implementation on a FPGA-based PMU Protoype

The proposed synchrophasor estimation algorithm has been fully deployed on a Virtex-5 FPGA. The PMU prototype is capable of processing 12 channels (voltages or currents) and estimate their related synchrophasor at the maximum reporting rates specified in the IEEE Std. C37.118-2011.





PXI-based system for the PMU metrological characterization

PMU prototype

Delta-Sigma converters for the sampling of the voltage and current waveforms

GPS unit for time synchronization

Compliance Verification with the Limits of the IEEE Std. C37.118.1-2011 and Conclusions

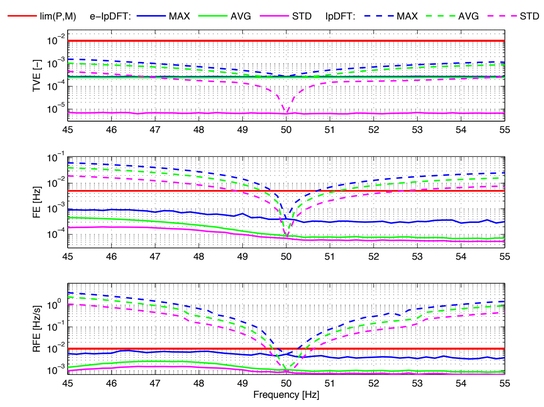
The experimental validation of the developed PMU has been carried out using reference waveforms generated by means of a GPS-synchronized function generator based on the PXI architecture.
Every test described in the IEEE Std. C37.118.1-2011 for both static and dynamic conditions was implemented. The results are given for both IpDFT and e-IpDFT algorithms with reference to TVE, FE and RFE limits for PMU classes P and M.

CONCLUSIONS

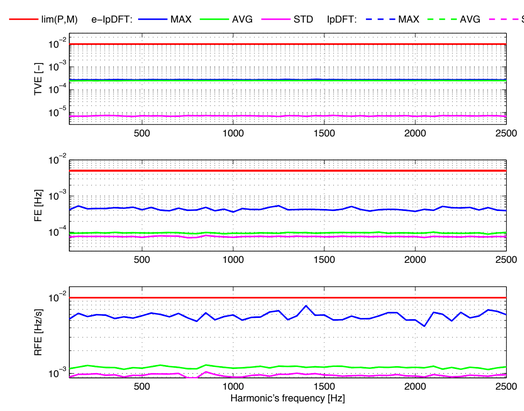
The proposed e-IpDFT-based algorithm introduces a remarkable improvement in the PMU performances, compared to those of the more classical IpDFT approach.
The obtained results show that the PMU prototype performs well below the limits imposed by IEEE Std. C37.118.1-2011 for both PMU classes M and P, enabling its use in several applications in transmission and distribution networks.

Static tests

Single-tone signals

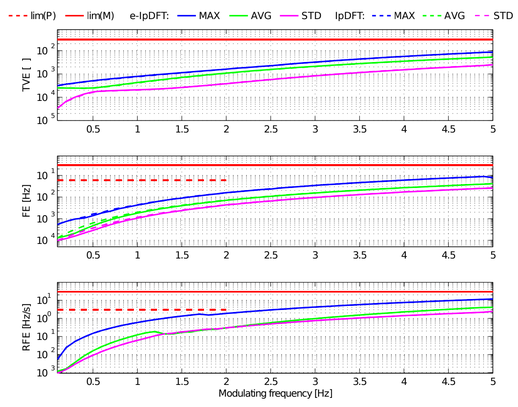


Multi-tone signals

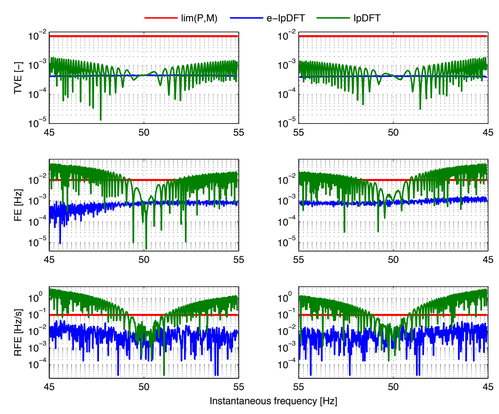


Dynamic tests

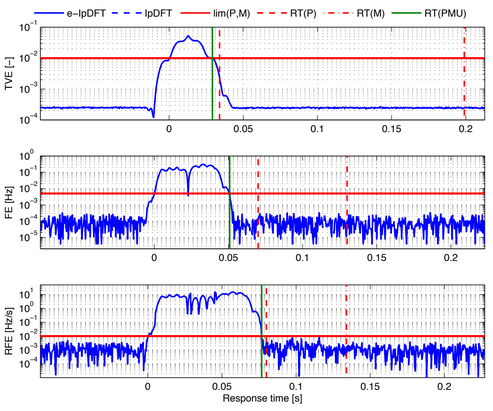
Amplitude-phase modulation



Frequency ramp



Positive amplitude step



Positive phase step