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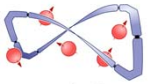
Novel MRI Platforms:
Massive Data Acquisition and Processing for very high channel count distributed receivers

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Wearable MRI

Motivation

We aim at enhancing existing and enabling new methods in magnetic resonance imaging (MRI) signal acquisition and processing such as scan acceleration, improved signal quality and more patient comfort by building high-channel count in-bore receiver electronics and massive data aquisition and processing units.
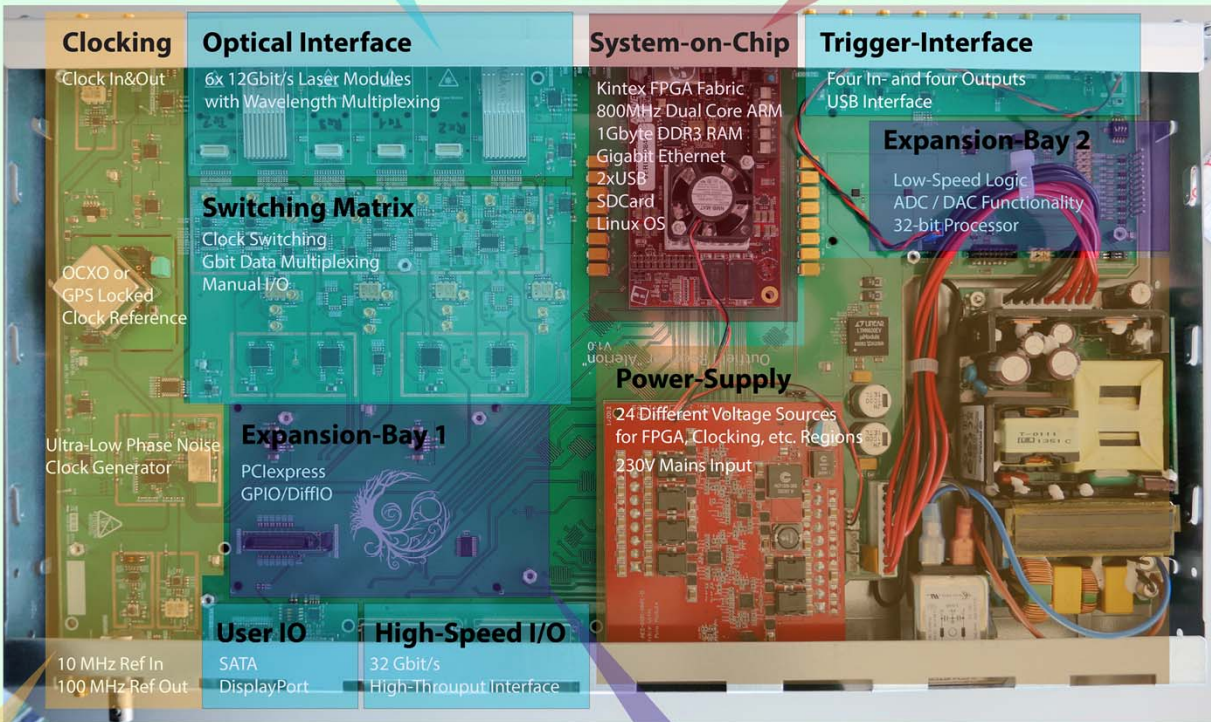
Design Overview

In order to collect and preprocess the data stream from the high channel count arrays the previously introduced data acquisition unit has been significantly expanded in its capabilities. The chosen architecture provides ample real time processing power for handling massive arrays as well as for future use in real-time accelerating tasks such as feedback of field measurements, motion detection and correction, fast channel combinations etc.

First images have been recorded using this new platform.

High Bandwidth Optical Reception/Transmission

The system hosts 4 x 12 Gbps Receive and 2 x 12 Gbps Transmit optical modules which can be connected to existing magnetic field compatible FPGA boards. Those boards can be used in conjuction with two 8-channel ADC boards offering a total count of 4 x 16 channels. However, it is designed to operate in parallel with further out-field receiver modules scaling the channel count accordingly. The same FPGA boards can be used as nodes to collect the data from several recently developed ASICs replacing the existing ADC boards.

Massive Data Processing System

The digital processing system is based on a Xilinx® Zynq®-7045 module hosting a 800 MHz dual-core ARM® processor and a Kintex®-7 FPGA. It is a powerful computing engine suitable for hardware accelerated, real-time and massive data processing. It is the module where all peripheral interfaces, high-speed optical modules and the high-bandwidth NI FlexRIO® interface are gathered together.

Clocking
Clock In&Out

OCXO or
GPS Locked
Clock Reference

Ultra-Low Phase Noise
Clock Generator

Optical Interface
6x 12Gbit/s Laser Modules
with Wavelength Multiplexing

Switching Matrix
Clock Switching
Gbit Data Multiplexing
Manual I/O

Expansion-Bay 1
PCIexpress
GPIO/DiffIO

System-on-Chip
Kintex FPGA Fabric
800MHz Dual Core ARM
1Gbyte DDR3 RAM
Gigabit Ethernet
2xUSB
SDCard
Linux OS

Power-Supply
24 Different Voltage Sources
for FPGA, Clocking, etc. Regions
230V Mains Input

Trigger-Interface
Four In- and four Outputs
USB Interface

Expansion-Bay 2
Low-Speed Logic
ADC / DAC Functionality
32-bit Processor

User IO
SATA
DisplayPort

High-Speed I/O
32 Gbit/s
High-Throuput Interface

10 MHz Ref In
100 MHz Ref Out

High-precision low-jitter clocking & synchronization

The unit hosts a high-precision oscillator clock with the possibility of GPS and external phase/frequency locking providing the reference clock which is distributed to the entire system as well as highly synchronized trigger I/O.

Extensions and Peripherals

The system supports a variety of extensions and perpheral interface standards such as SATA, HDMI, USB, Ethernet, PCIe and general purpose IOs. The outfield receiver system interfaces further primarily to a NI FlexRIO® system. However, the system can opperate fully autonomously.