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WearMeSoC RTD 2013

FNSNF

Development and Optimization of a System-on-Chip (SoC) for Portable Medical Instrumentation

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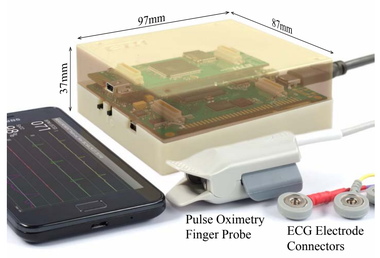
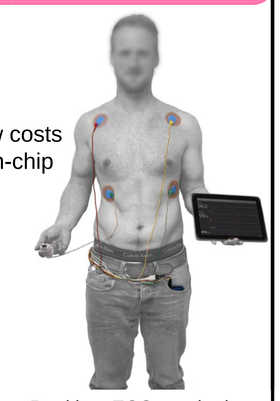
Portable and Wireless Medical Instrumentation

Clinical & Point-of-Care Devices:
- Provide uncompromised biosignal acquisition and processing quality, but:
  - High cost and power consumption
  - Not portable

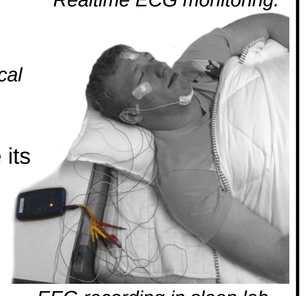
Portable Device with Wireless Link:
- Need to trade off medical-grade signal quality against:
  - Size (form factor)
  - Ultra-low power consumption & low costs
  - Multi-sensor support with limited on-chip signal processing resources



Highly flexible, modular, and portable medical instrumentation device with wireless link.



Realtime ECG monitoring.



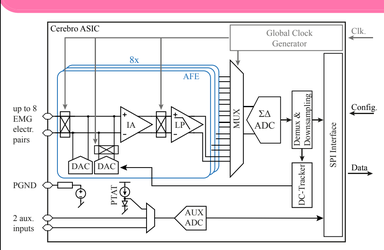
EEG recording in sleep lab.

Objective: Develop technologies essential to miniaturize wireless monitoring, and demonstrate its effectiveness in real medical use cases

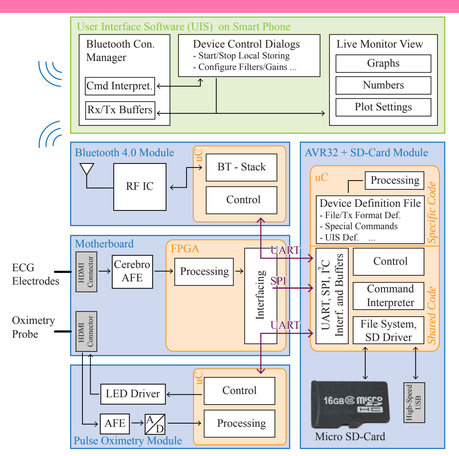
Motivation: Aging population, escalating medical costs, silent suffering, illness prevention

Problems: High complexity, too diverse applications, target device size limits battery capacitance, low amplitude signals, electrical noise and distortions

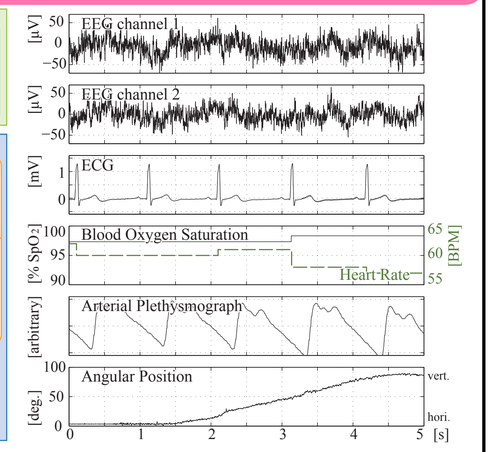
HW Development and Optimization using a Modular and Flexible Platform



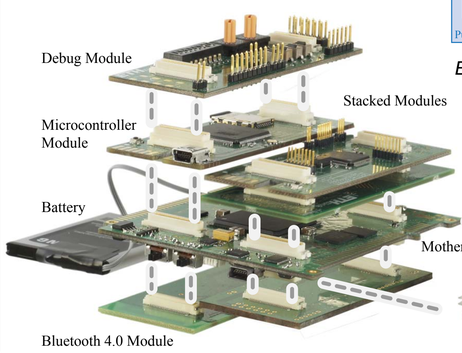
Cerebro: Biomedical data acquisition ASIC supporting ECG, EMG, EEG, EOG, ... Chip developed at IIS (ETH Zurich). A signal bandwidth of 3.2kHz is offered with DC signal tracking [3].



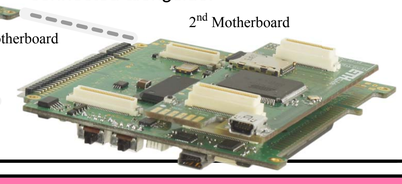
Block diagram of the modular platform.



Biomedical signals recorded with the prototype to be used in sleep research. It includes multiple EEG channels ECG, pulse oximetry, and angular positioning.

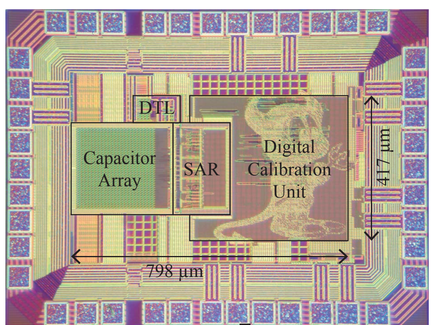


Up to 6 daughterboards can be plugged on one motherboard - multiple motherboards can be connected alongside.

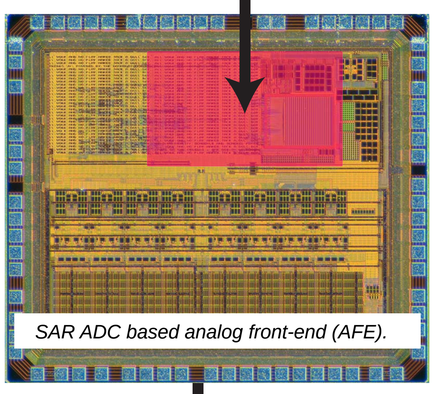


Development Platform [1]:
- Modular
- Flexible
- Programmable
- Multi-sensor support
- Wireless link capability
- Cost efficient HW development

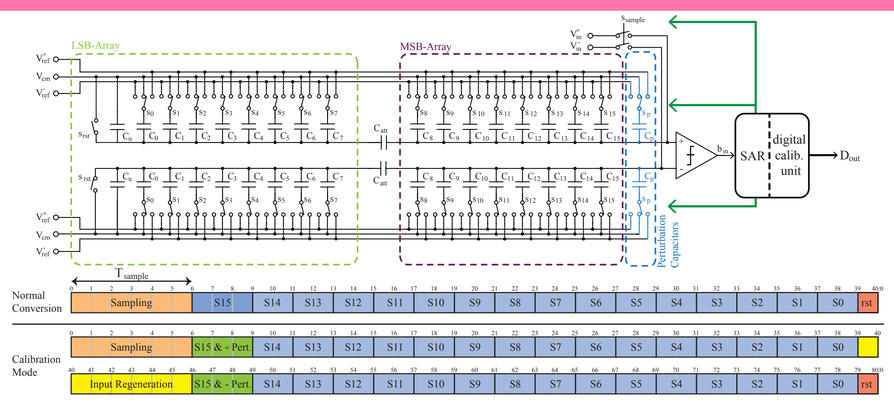
Our Solution: Programmable ADC with On-Chip Calibration Circuitry Resolving 8-14 Bits for Multi-Sensor Support



Micrograph of SAR ADC.



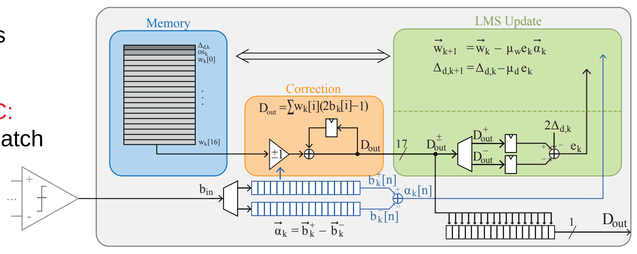
SAR ADC based analog front-end (AFE).



Schematic of the 14-bit sub-radix-2 SAR ADC with merged capacitor switching scheme (top) and corresponding timing diagram (bottom).

SAR ADC:
- Performs dithering techniques to enhance resolution
- Sub-radix-2 capacitor array
- Programmable from 8-14 bits
- Ultra-low power operation

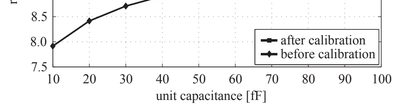
Digital Calibration of SAR ADC:
- Correction of capacitor mismatch
- LMS based algorithm
- Perturbation injection
- On-chip implementation
- Improvement: 1.8 ENOB



Block diagram of LMS based digital calibration unit.

Advantages of the programmable SAR ADC:
Power consumption can be tuned against precision, low power consumption, small die size, high precision, 13.5 ENOB achieved with dithering techniques

Conclusion:
SAR ADC based analog front-end ASIC successfully tested with real-world biomedical signals



Fixed-point Matlab simulation of the SAR ADC resolution before and after calibration for different unit capacitors using 1000 Monte Carlo simulations.

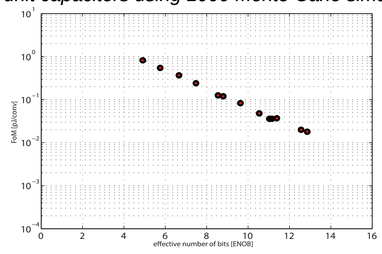
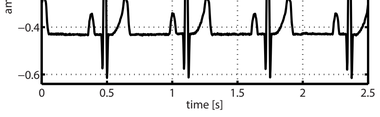
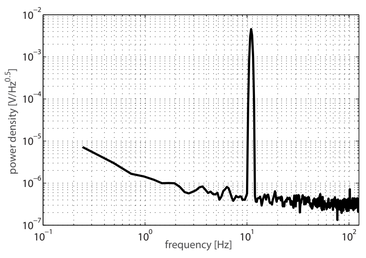


Figure-of-Merit (FoM) versus ENOB of our SAR ADC implementation. ADC ranges from 8-14 bits of resolution with max.12.7 ENOB.

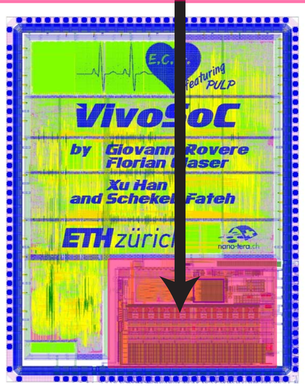


Recorded ECG signal with the SAR ADC based analog front-end ASIC.



FFT of a recorded 11 Hz sinusoidal signal with the SAR ADC based analog front-end ASIC representing a typical EEG signal spectrum.

VivoSoC: Ultra-Low-Power Processing (PULP) Platform with AFE

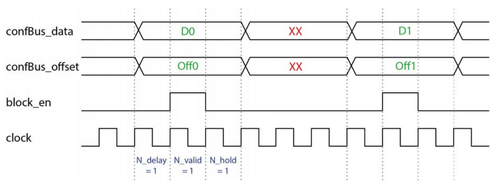


Area:	4.0 mm x 3.2 mm
Technology:	130 nm CMOS (tapeout: April 2015)
Architecture:	Dual core RISC 2kByte Cache, 32kByte L2, 16kByte TCDM
Analog Front-end:	8 multiplexed channels with 108 dB CMRR and 3.2 kHz signal bandwidth
Peripherals:	• 2 quad SPI masters • 1 SPI slave • 8 GPIO, 1 JTAG • 1 UART

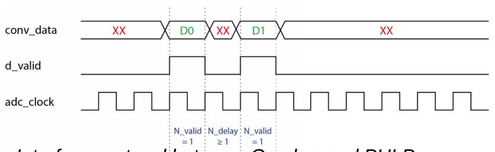
Chip layout of VivoSoC and corresponding key features.

VivoSoC:
- Supports trend of miniaturization
- Ultra low power consumption
- Robust operation
- Controlled over wireless interface
- Supports readout of biomedical data
- Signal processing capability

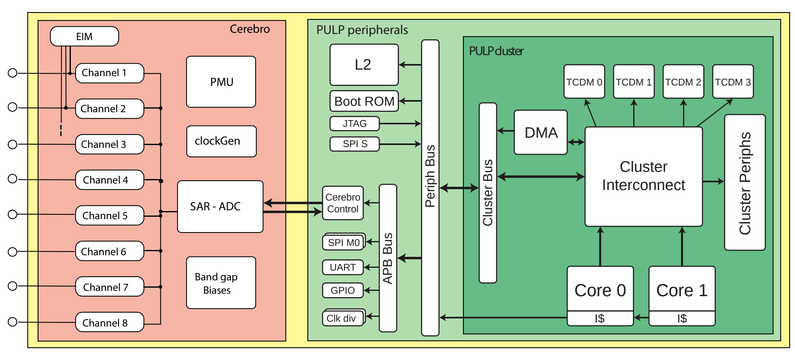
PULP [2]:
- Configurable, feature rich, power-saving digital signal processing platform
- Built on a dual core RISC processor
- Easy-to-use, extendable, and robust interface
- Enable configuration and readout of AFE
- One core only for wireless control and protocol stack



Interface protocol between Cerebro and PULP to configure the analog circuitry software based.



Interface protocol between Cerebro and PULP to read out data using a valid signal.



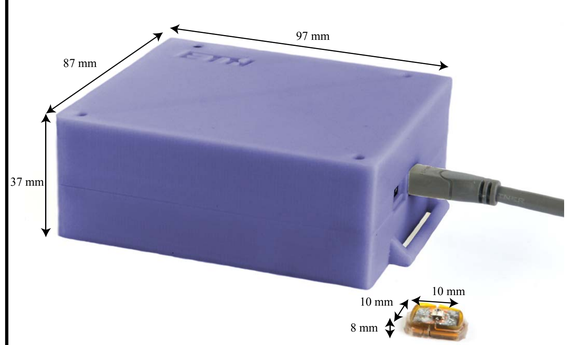
Block level schematic of VivoSoC: PULP combined with AFE on a single die.

Conclusions and Outlook

Conclusions:
- Successful tests of the modular platform by medical partners
- Implementation of a programmable SAR ADC to cover efficiently different biomedical application
- SAR based AFE trades low power consumption against precision
- Ultra-low power System-on-Chip for biomedical data acquisition platform called VivoSoC implemented

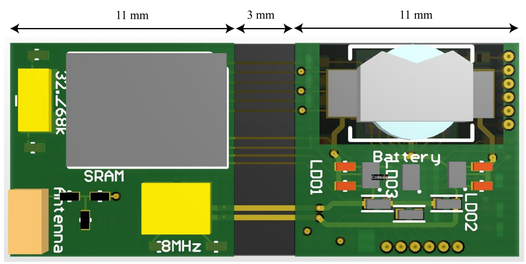
Outlook:
- Additional track in implantable devices
- Targeted device size below 0.8 cm^3
- Directly interfacing nerves instead of skin contact
- Stimulation of nerves also feasible

Implantable device wirelessly controlled with mobile device.



Dimensions of modular biomedical device versus implantable system.

6 Layer Rigid-Flex-Rigid PCB with Thickness of 0.8 mm



Implantable device acquires data and forwards them to the low-energy Bluetooth device. A RAM is used to buffer data. The device consists of two PCBs connected through a flex-print and is folded to minimize device dimensions.

References:

[1] P. Schönle et al., "*Modular multi-sensor platform for portable and wireless medical instrumentation*", Proc. IEEE BioCAS, Oct. 2014.

[2] F. Conti et al., "*Energy-efficient vision on the PULP platform for ultra-low power parallel computing*", Signal Processing Systems (SiPS), Oct. 2014.

[3] P. Schönle et al., "*A DC-connectable biomedical data acquisition ASIC with mains frequency cancellation*", Proc. IEEE ESSCIRC, Sept. 2013.