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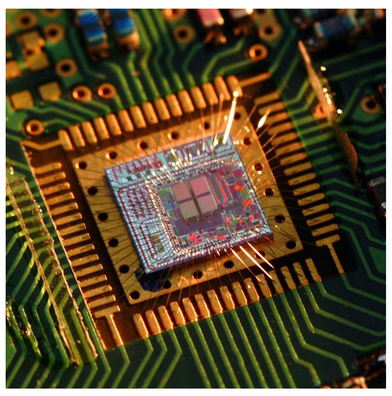
icySoC RTD 2013

FNSNF



Ultra low power processing based on a sub-threshold implementation

M. Pons[1], D. Séverac[1], J-L. Nagel[1], D. Ruffieux[1], S. Emery[1], P. Rochaix[2]

[1] CSEM SA, [2] EM Microelectronic-Marin SA

csem
info@csem.ch www.csem.ch

em

The main goal of sub- or near-threshold design (i.e. integrated circuits supplied with a voltage lower or just above MOS transistor threshold voltage) is to reduce the dynamic power consumption (and therefore the energy per cycle in a processing circuit) by decreasing the supply voltage. At these low voltages, digital standard cell libraries and memories need to be revisited to ensure integrated circuits correct operation. A standard cell library as well as memory blocks have been designed in EM Microelectronic Marin ALP 180 nm technology. Those building blocks have been used for the design and integration of a CSEM 32-bit icyflex2 processor system. Corner lot measurements show robust operation of the circuit over process, voltage and temperature, reaching a minimum supply of 0.37 V and a minimum energy per cycle of 17.1 pJ/cycle. The 32-bit icyflex2 processor system is in fact able to work supplied by a single PV-cell. The integration therefore validates the design of the building blocks and demonstrates the capabilities of sub- and near-threshold techniques.

EM Microelectronic Marin ALP 180 nm sub-threshold building blocks

- Sub-threshold building blocks have been developed for designing complete ultra low power systems using a single power supply domain.

ROM building block

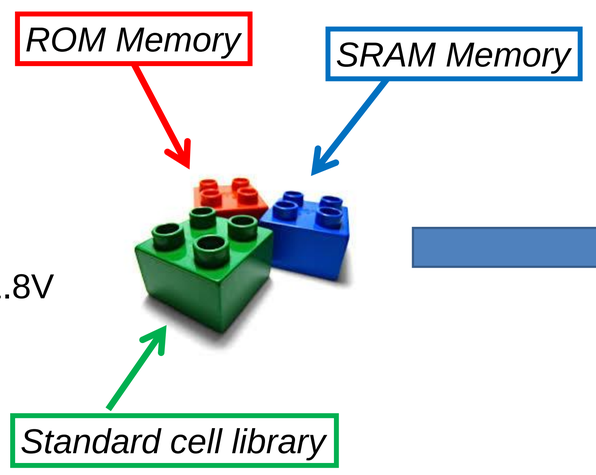
- Power supply range: 0.54V to 1.8V
- Size: 2048 bytes

RAM building block

- Power supply range: 0.54V to 1.8V
- Size: 256 bytes
- Bit-cell: 6T

Standard cell library

- Power supply range: 0.54V to 1.8V
- L=300nm
- 72 cells

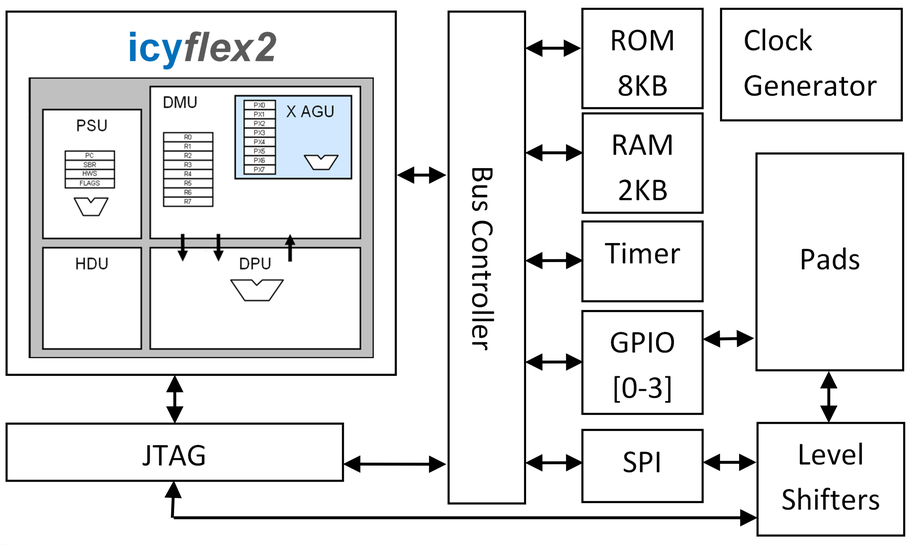


Complete sub-threshold design

- Power supply range: 0.54V to 1.8V

  → Single power domain

CSEM 32-bit icyflex2 processor system



icyflex2 system description

- The icyflex2 core is composed of four distinct units:
  - The program sequencing unit (PSU)
  - The data move unit (DMU)
  - The data processing unit (DPU)
  - The host and debug unit (HDU)
- The system includes GPIO, JTAG, SPI and Timer peripherals.
- Optimized high range level shifters are inserted in pads.

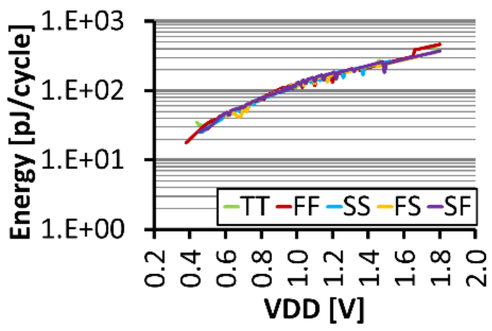
icyflex2 system evaluation

- Software self-test (MBIST) of RAM, using March C algorithm.
- MBIST executed by the icyflex2 core from the ROM, without support from the RAM → test for all building blocks.
- Passed or failed test is output on the GPIOs.

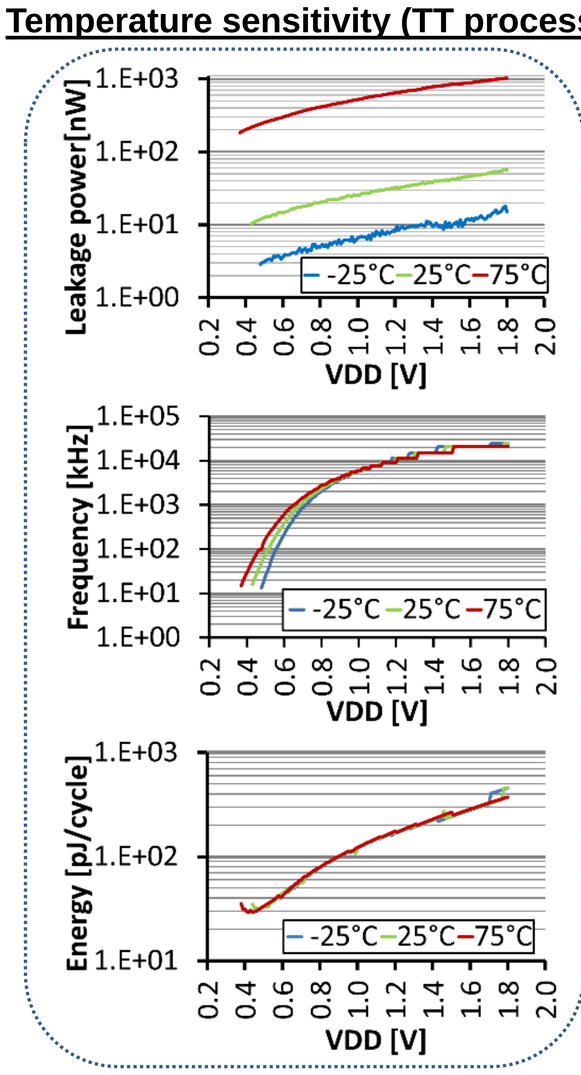
Integration measurement results

Micrograph of the test chip. The equivalent gate count of the icyflex2 core is 40 kgates.

Corner lot measurements



Temperature sensitivity (TT process)



Main results

- Robust operation over process: TT, SS, FF, SF, FS (corner lot)
- Robust operation over temperature: -25°C to 75°C
- Robust operation over a wide supply range: 0.37V to 1.8V
- Minimum energy per cycle of 17.1 pJ/cycle
- Tested to work directly on a PV-cell (enables energy harvesting)