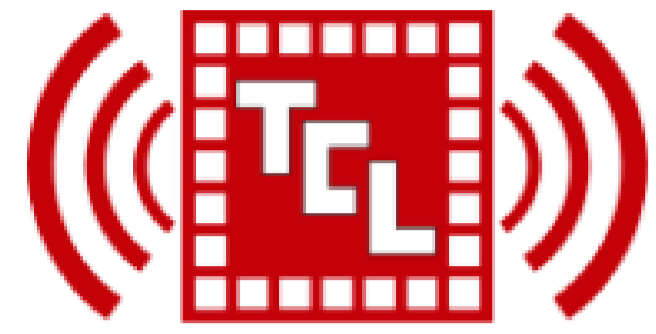


Multipliers-Driven Perturbations of Coefficients for Low-Power Operation in Reconfigurable FIR Filters



Telecommunications Circuits Laboratory (TCL), École Polytechnique Fédérale de Lausanne (EPFL)

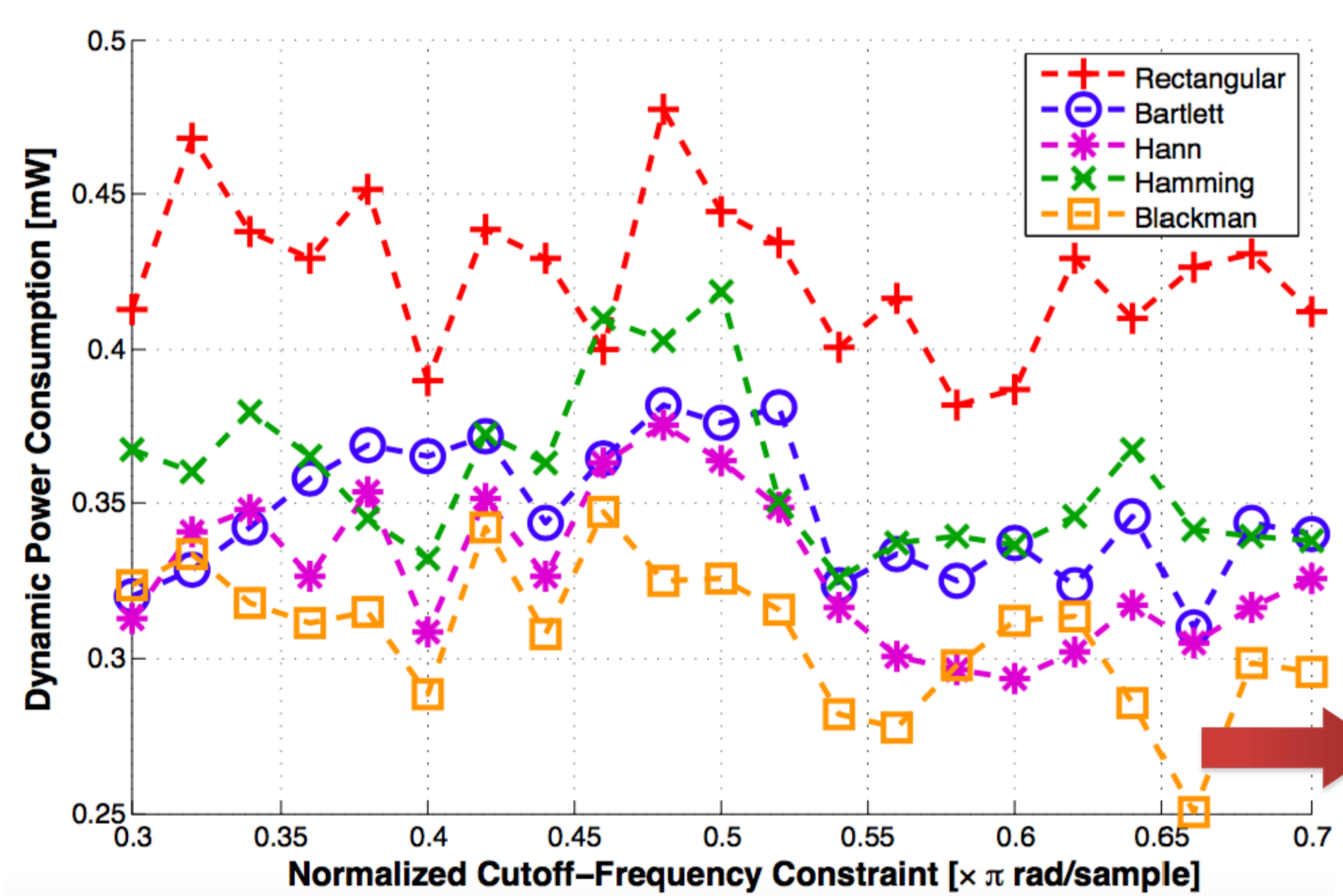


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Low-Power Digital Signal Processing

Portable devices require digital signal processors able to:

- Support different communication standards
- Ensure a long battery life



Reconfigurable FIR filters are widely implemented and it is essential to limit their power consumption.

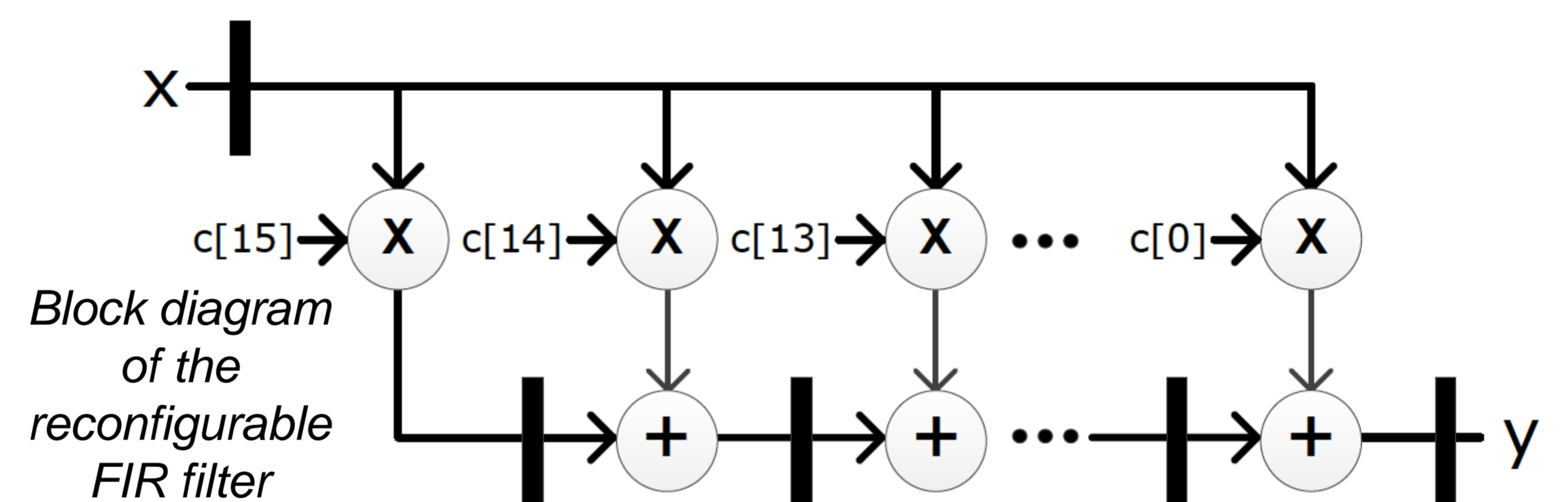
Dynamic power significantly varies in multipliers with design constraints and windowing method.

Dynamic power of the 8x8-bit multipliers in a 16-taps FIR filter

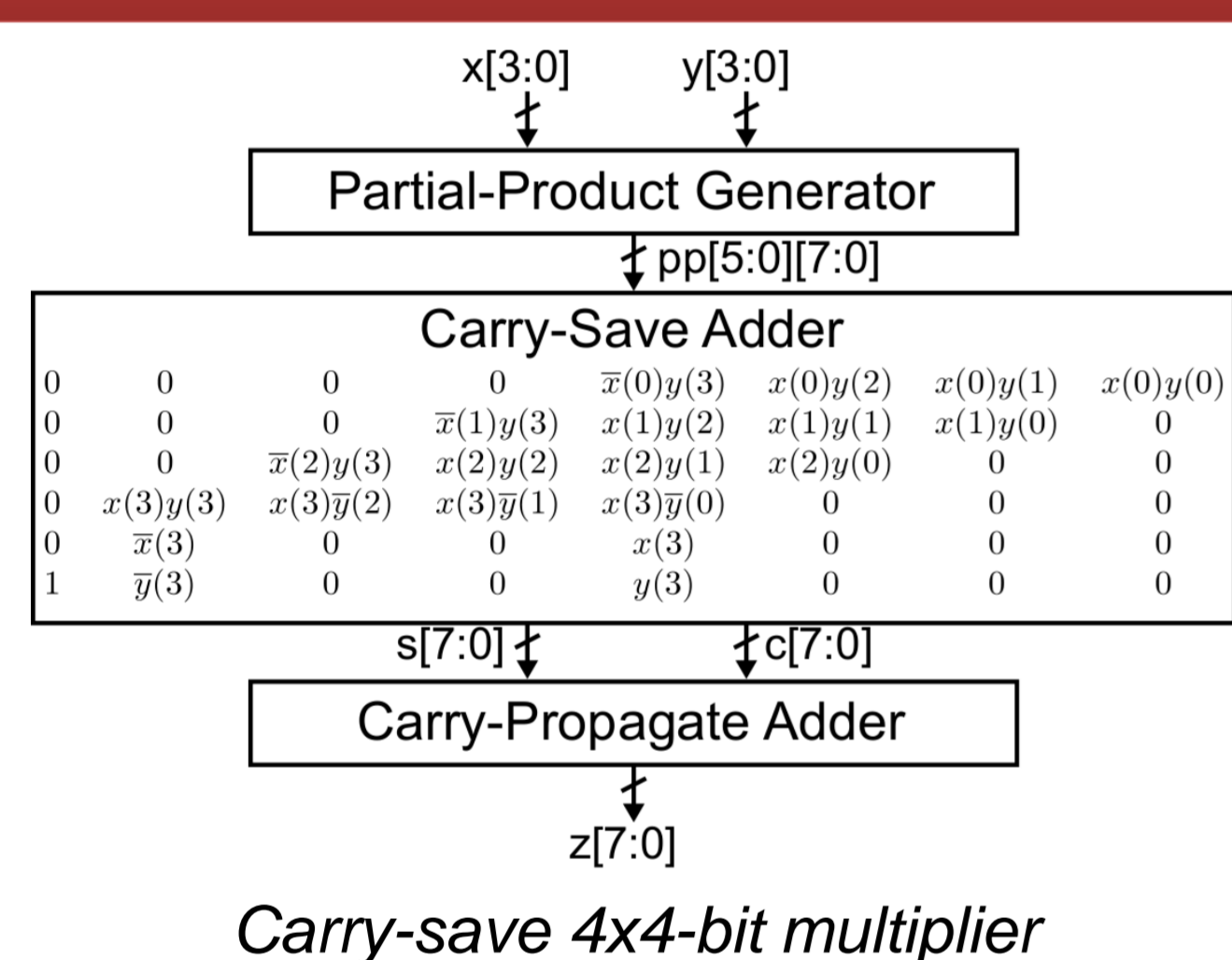
Perturbation of FIR Coefficients

Coefficients in FIR filters are perturbed for low-power operation:

1. **Reconfigurable FIR filters** are considered where different coefficients can be assigned to the multipliers
2. **Analysis of switching activity** conducted in common multipliers to identify possible dynamic-power savings
3. **Gate-level power simulations** of multipliers for an accurate characterization of the possible power savings
4. **Perturbation of exact FIR coefficients** to trade accuracy of the filter for less power consumption



Switching Activity in Multipliers

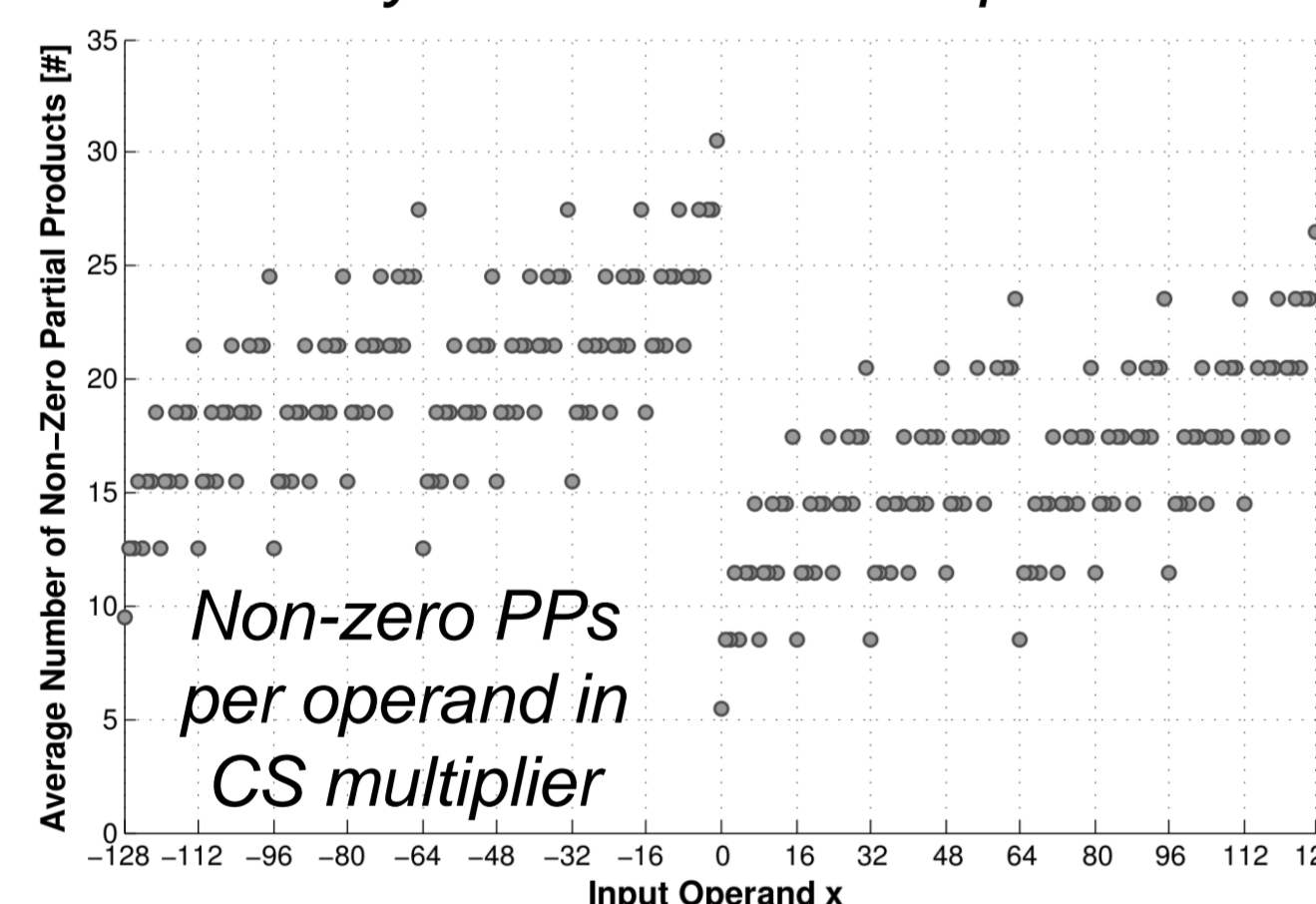


Reduce dynamic power:

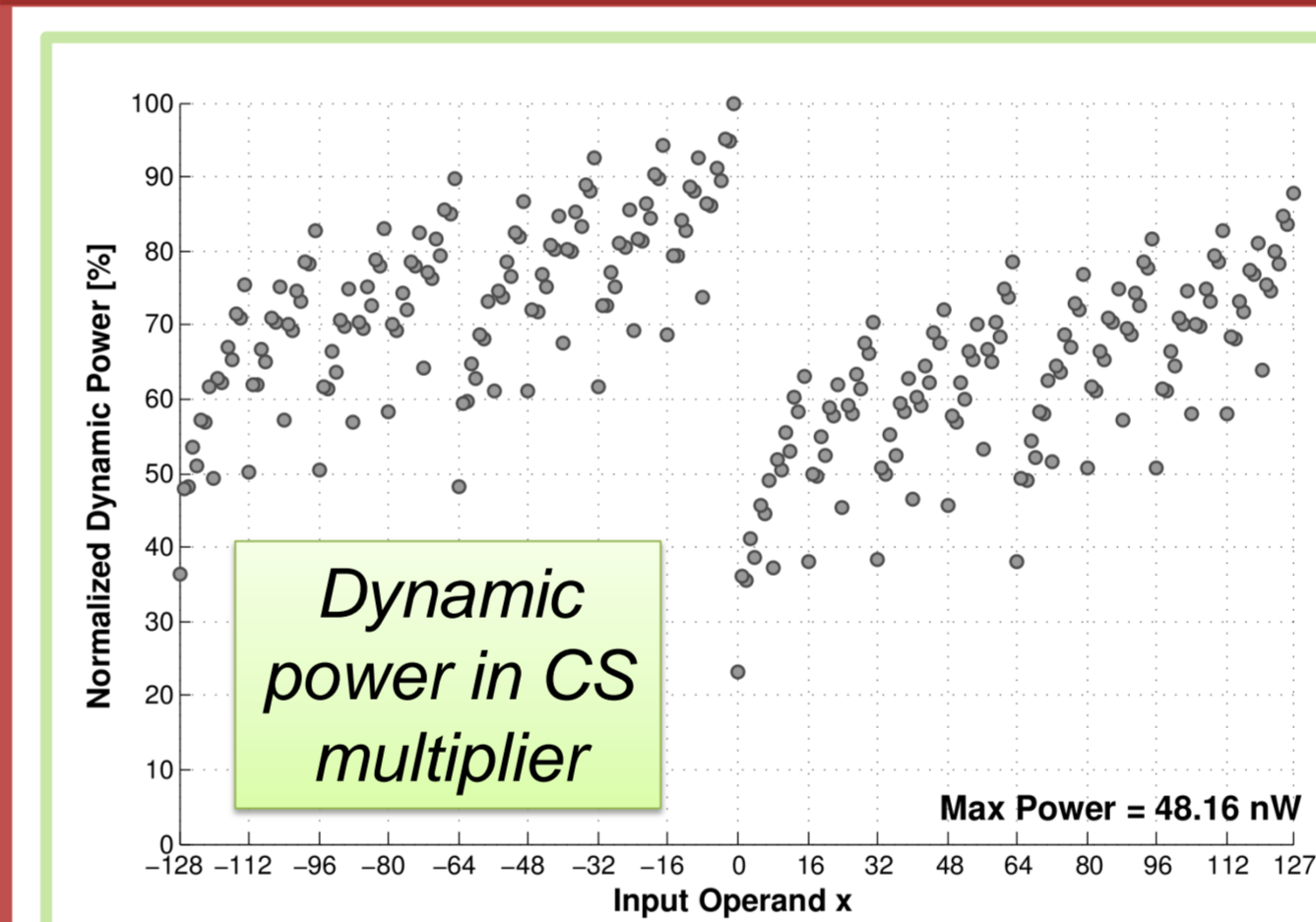
- Limit switching activity in the carry-save adder.
- Find operands that minimizes the number of non-zero partial products (PPs).

Carry-Save (CS) Multiplier

- Simple and medium speed
- **Symmetric**: power savings given for both input operands
- **Radix-4 Booth (BR4) Multiplier**
- Complex and high speed
- **Asymmetric**: savings given when assigning coefficients to the recoded operand

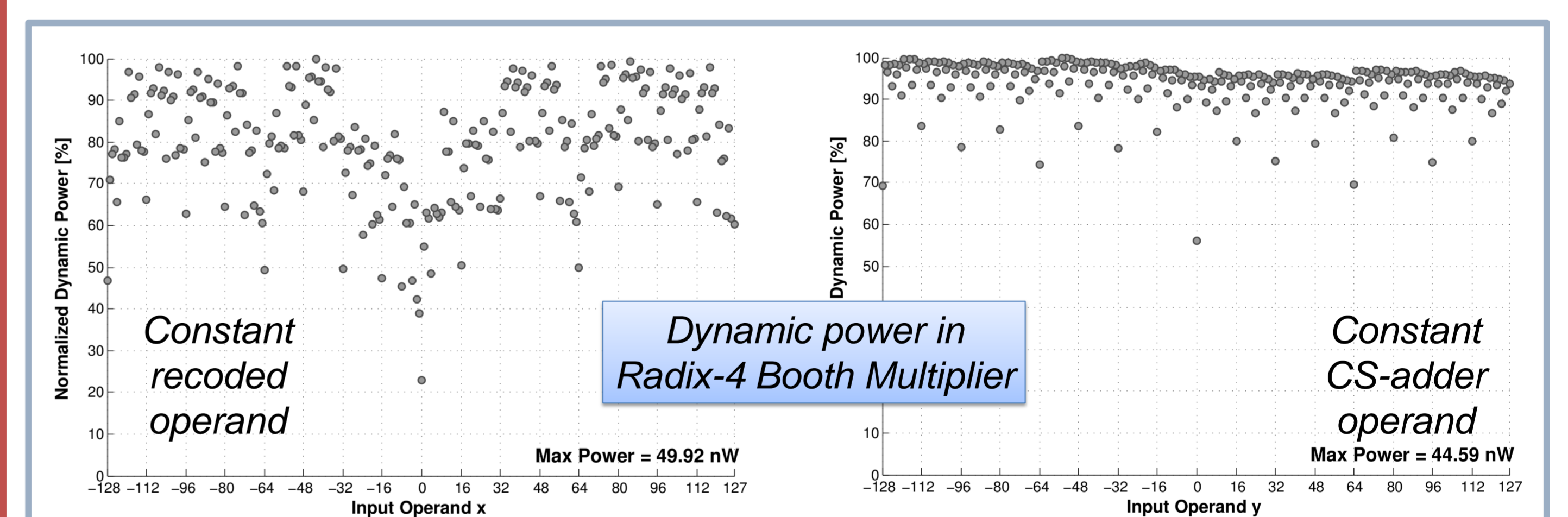


Gate-Level Characterization of Multipliers

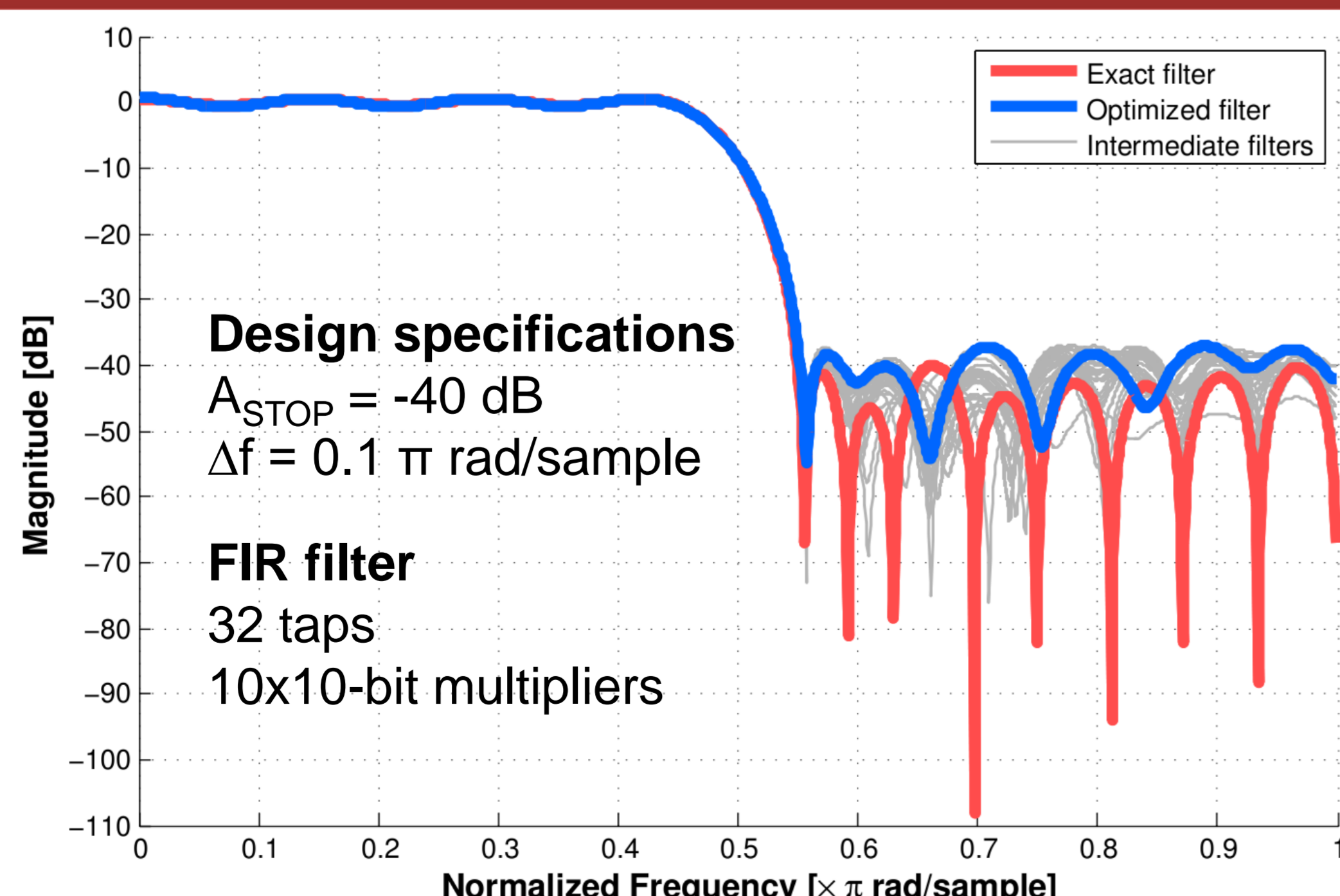


Gate-level simulations

- Accurate power characterization
- Confirmed expected savings
- Preferring the operand that allows for power savings does not affect the multiplier speed



Response of the Approximated FIR Filter



Design specifications
 $A_{STOP} = -40$ dB
 $\Delta f = 0.1 \pi$ rad/sample

FIR filter
32 taps
10x10-bit multipliers

- The exact coefficients are perturbed based on multiplier characterization to maximize the power savings.
- Approximated filter obtained accepting only 3dB error on stopband attenuation to minimize accuracy degradation

Power Savings and Conclusions

TABLE II
DESIGN SPECIFICATIONS AND POWER SAVINGS OF THE FIR FILTERS

A_s^a [dB]	F_c^a [π rad/sample]	Multipliers Width	Taps	S_{Mul}^b [%]	S_{FIR}^b [%]
-30	0.2	8x8	16	18.0	14.7
-40	0.2	10x10	16	24.2	19.5
-30	0.1	8x8	32	24.2	20.2
-40	0.1	10x10	32	14.6	11.7

^a Design specifications of the exact filter.

^b Obtained when tolerating a 3 dB error on the stopband attenuation.

Power savings in the FIR filter

- Coefficients perturbation verified on different FIR filters
- Dynamic power savings:
 - Up to **24.2%** in multipliers implemented in the filter
 - Up to **20.2%** in FIR filters due to design overhead

Conclusions

- **Exact operation** preferred when accuracy required
- **Approximated coefficients** used for low-power operation