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IcySoC RTD 2013

FNSNF

IcySoC Ultra Low Power Design with Approximate Computing

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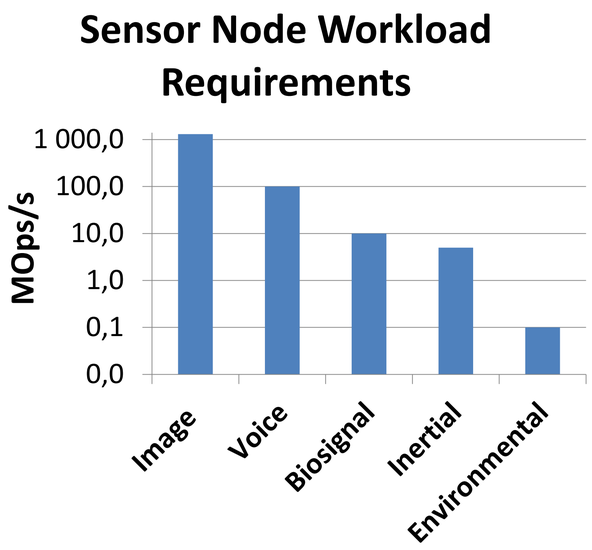
CSEM, EPFL ICLAB, ETHZ, EPFL TCL, EM Microelectronics

Motivation: Strong need for energy-efficient *near sensor processing* of data *with very different workloads*

- Wearable Health Monitoring
- Environmental Monitoring and Automated Surveillance
- Implanted Medical Devices
- Internet of Things
- Personal Electronics
- …



IcySoC Mission: Develop technologies for the design of ultra-low-power computing platforms that *maintain energy efficient operation over a wide range of application/processing requirements*

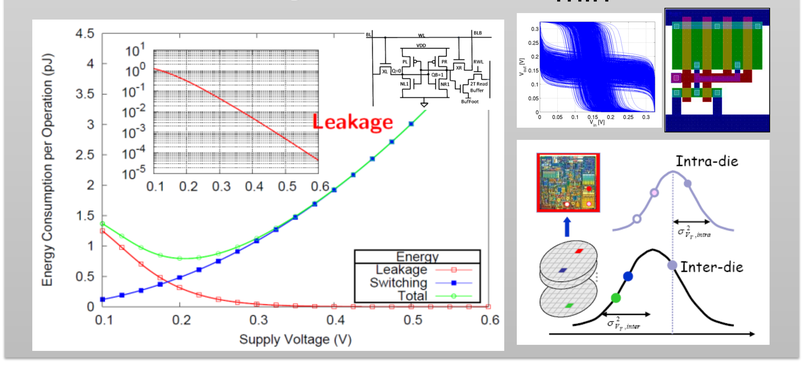
Technology Ingredients, Challenges, and Solutions

Technology & Circuits

ULP design and energy proportionality through near- and sub-Vt operation

Challenges:

- Energy efficiency limited by leakage power
- Process variations increase uncertainty & limit reliability
- Reliability limits Vdd_{min}

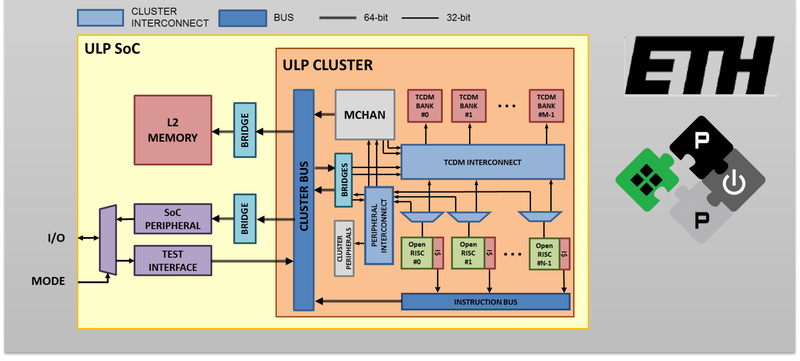


System & Architecture

Smart multi-core platform (PULP) designed specifically for operation at low voltages

Challenges:

- Efficiently support different workload requirements
- Architectural measures to compensate for variations
- High performance at low Vdd

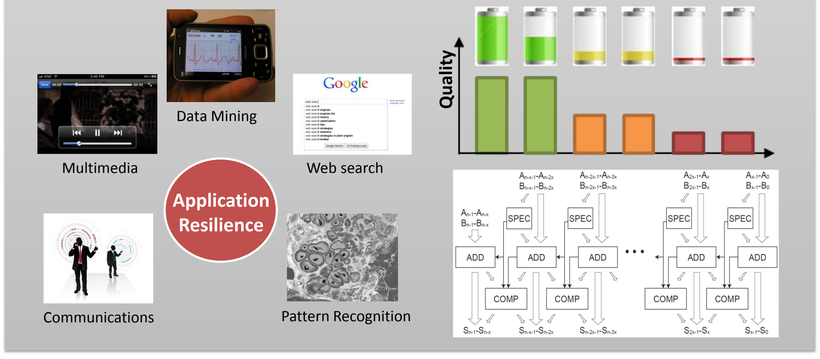


Approximate Computing

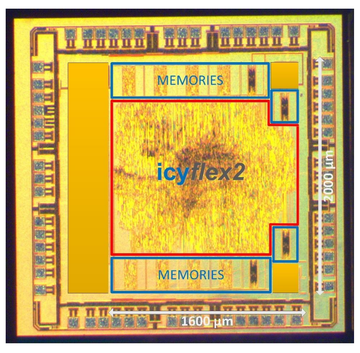
A new paradigm that exploits tolerance of many applications to inaccuracies to reduce complexity

Challenges:

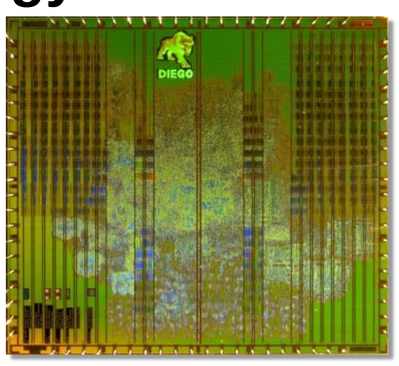
- Maximize complexity savings for minimum QoS degradation
- Graceful QoS degradates with user demands
- Circuit design and test



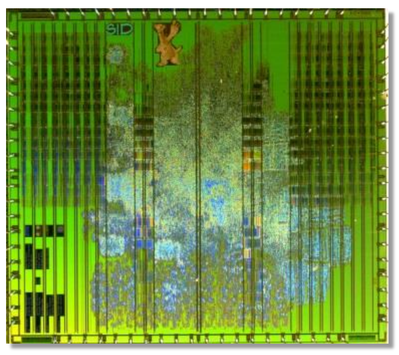
Some technology demonstrators and testchips developped in the IcySoC project:



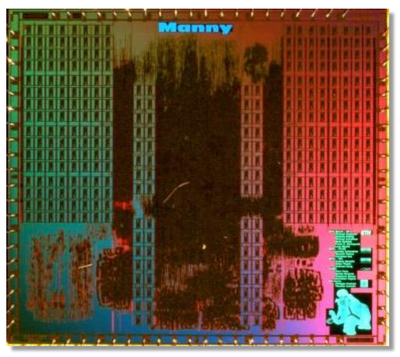
IcyFlex in 180nm



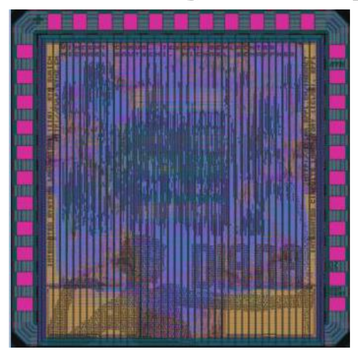
PULP in 180nm



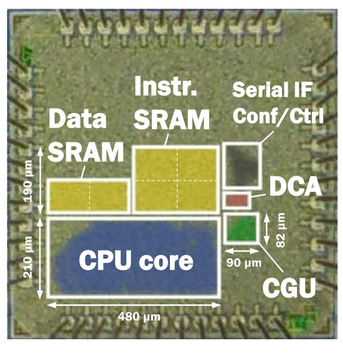
PULP in 180nm



PULP in 180nm



PULP in 65nm



dynOR in 28nm

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