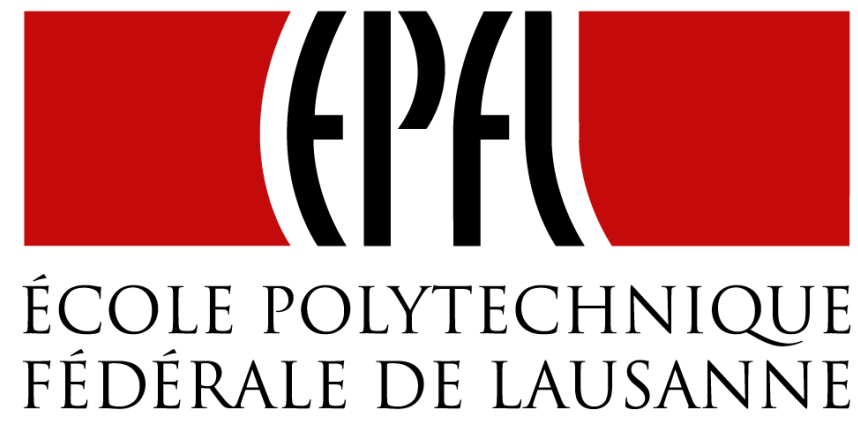


# Safe and Optimal Deployment of 3D Ultrasound Application on Kalray MPPA-256 Platform



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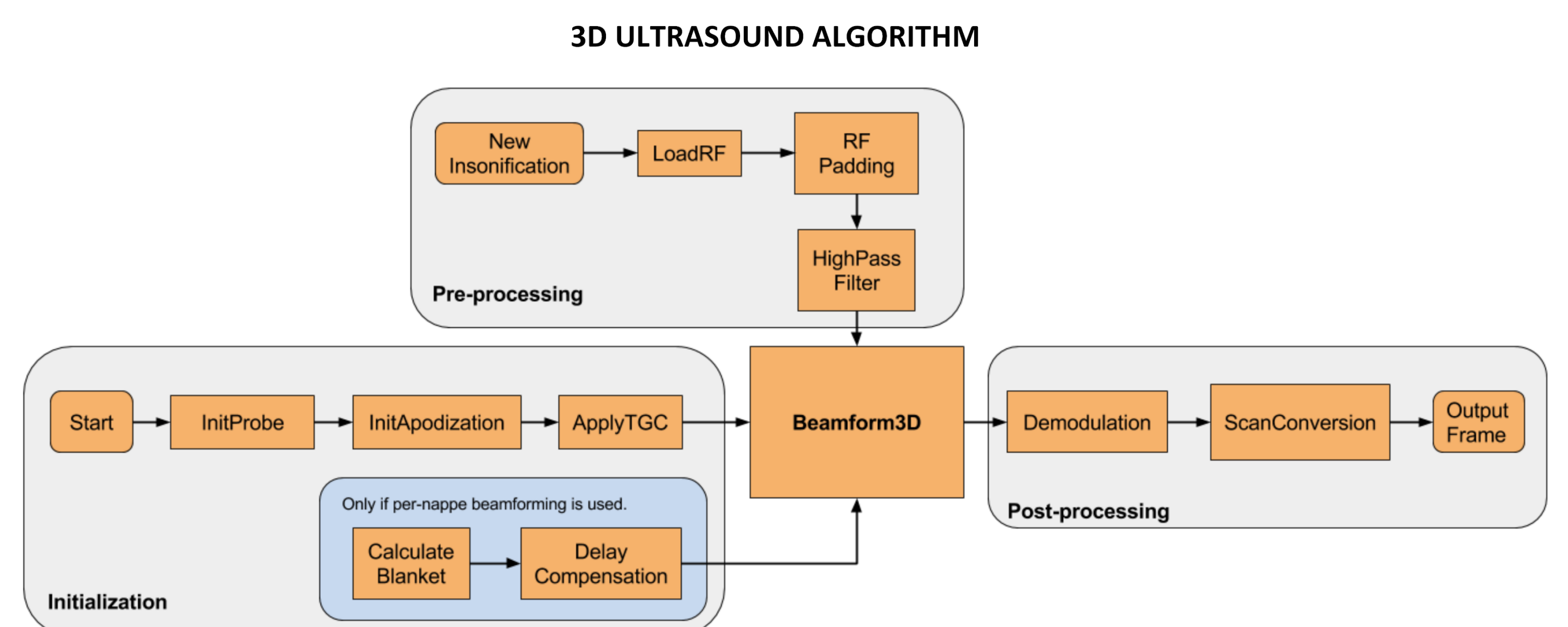
## Introduction

The optimal deployment of data streaming application onto many-core architecture is a multi-criteria optimization problem [1]. We solve this problem for 3D Ultrasound (US) application [2] with its most computationally demanding *beamforming* part being executed on MPPA-256 many-core chip with high degree of parallelization. The amount of shared memory on each cluster is limited (~1MB for application data), therefore we choose suitable optimal configurations of the US system.

## Safe and optimal US application deployment

### Steps of Ultrasound processing

- Generated of RF data by Field II simulation
- Initialization of essential US coefficients
- Highpass filtering of incoming RF data
- 3D beamforming by apodization and summing:
  - Beamforming is done nappe-by-nappe [3]
  - Delays are calculated on-the-fly by steering method
- Demodulation, scan conversion & visualization

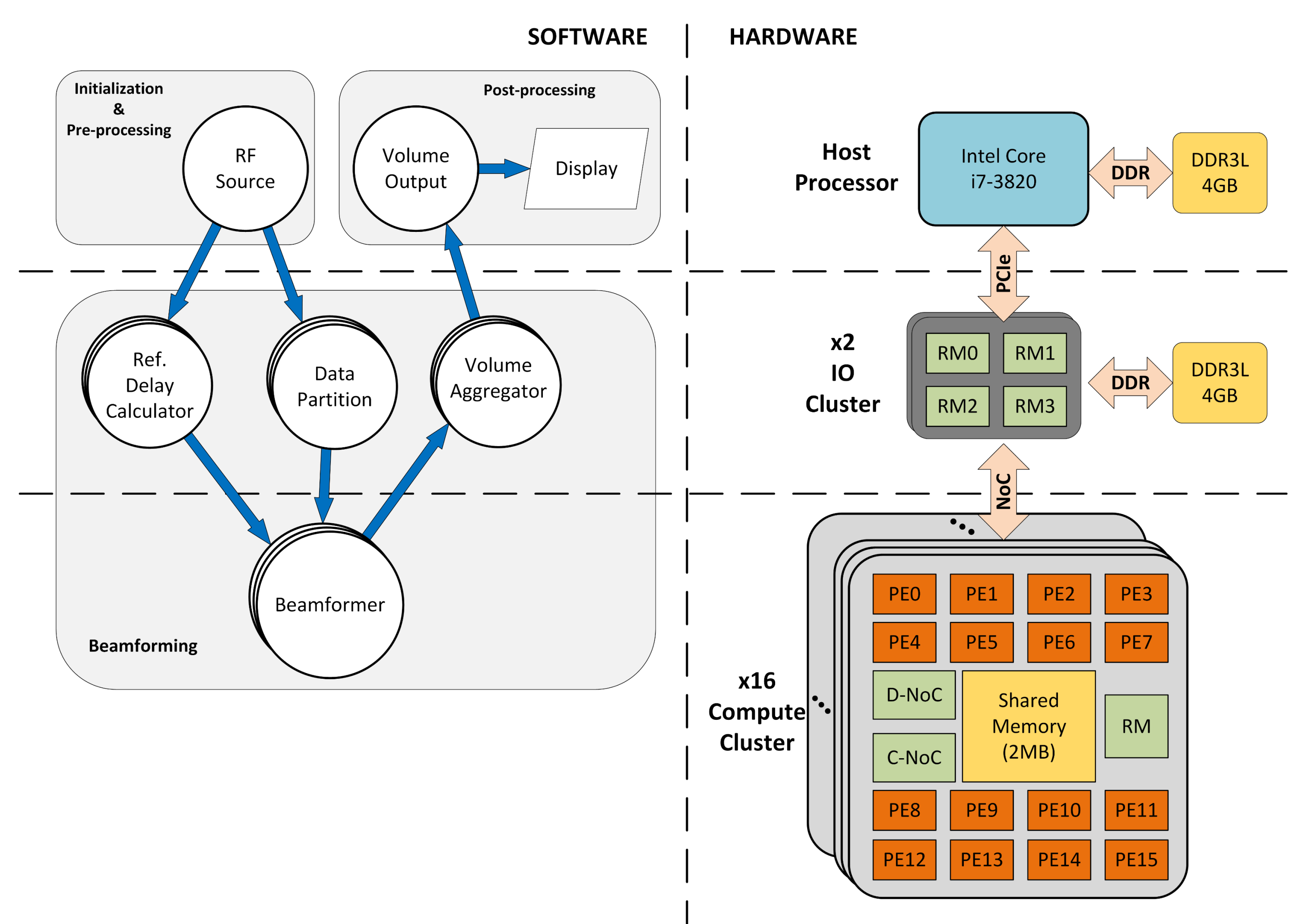


### Kalray MPPA-256 platform:

- Host processor Intel with 4GB DDR memory
- 2 IO clusters with 4 cores and 4GB of memory
- Many-core MPPA-256 chip:
  - 256 cores (400 MHz) in 16 clusters
  - 2MB shared scratchpad memory
  - 2D-torus NoC

### Software Implementation

- Initialization & pre-processing on Host
- Reference delays computed on IO clusters
- RF data partitioned on IO cluster
- Beamforming efficiently parallelized on compute clusters of Kalray MPPA-256 chip
- Output image is aggregated on IO clusters
- Scan conversion is done on Host



## Two memory-wise optimal configurations

- Probe = 12 x 12 array;
- Volume depth = 4.5cm
- $\varphi, \vartheta \in [-38^\circ, 38^\circ]$ ;
- $f_c = 4\text{MHz}$ ;
- $f_s = 200\text{MHz}$

A blanket of echo signals that need to be stored on each cluster:

Memory required by one blanket is ~ 1MB

Time running the whole application of the host processor (1 thread):

➤ ~ 30s      ➤ ~ 13 minutes

Time when Beamforming is running on the Kalray MPPA-256 chip:

➤ ~ 0.5s      ➤ ~ 14s

- Probe = 64 x 64 array;
- Volume depth = 4.5cm
- $\varphi, \vartheta \in [-38^\circ, 38^\circ]$ ;
- $f_c = 4\text{MHz}$ ;
- $f_s = 12\text{MHz}$

## Conclusion

- The memory usage is a trade-off between the probe size and sampling frequency
- The computation time is proportional to the probe-size and does not depend on the sampling frequency
- The acceleration gain in average is about 55 times

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