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WearMeSoC RTD 2013

FNSNF

Power Management Unit (PMU) for Wearable Medical Instrumentation

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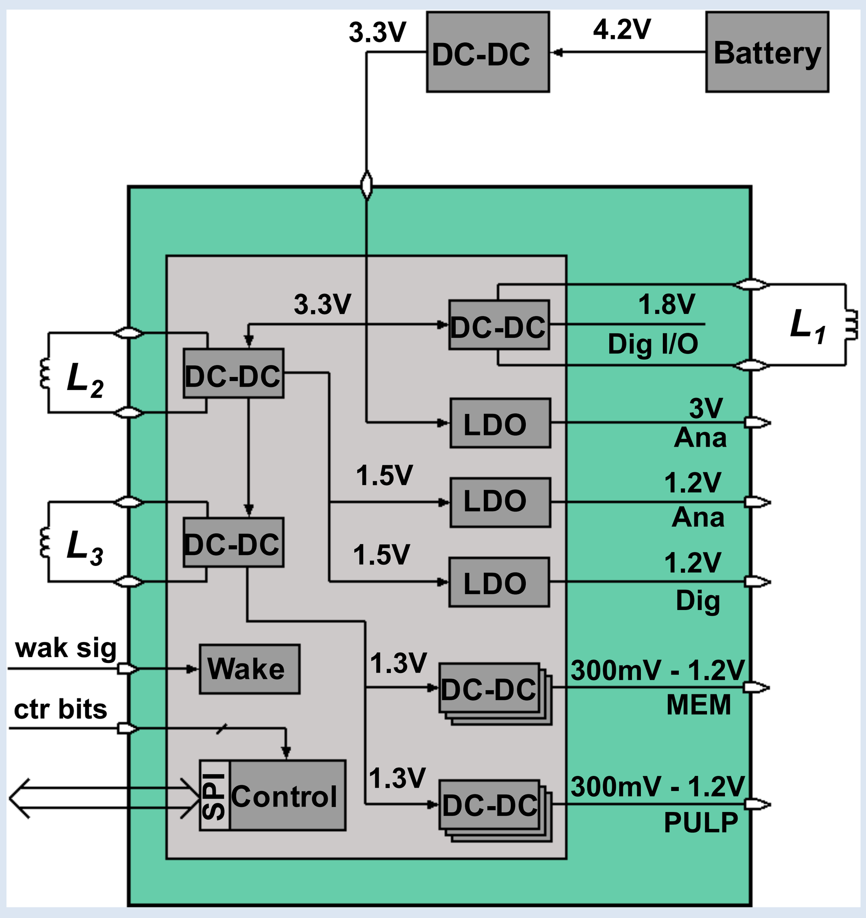
Abstract – Wearable medical instrumentation is becoming a hot commodity. Since size and weight prevent it from being widely used in the convenient and flexible way, highly integrated system on a chip (SoC) is required in the future ubiquitous biomedical instruments. On top of that, an on-chip PMU is the key solution to power the system in a wide range of applications. This work presents a PMU system designed for the VivoSoC project which can monitor different kinds of biomedical siganls (ExG).

1. PMU V1.0 System Overview



Output pin	Power level Sleep / Averaged / Max	Characteristics
Dig I/O	10uW / 2mW / 20mW	1.8V digital I/O power supply
Ana	1uW / 5mW / 15mW	1.2V analog power supply
Dig	1uW / 5mW / 15mW	1.2V digital power supply
Ana	5uW / 12mW / 30mW	3V analog power supply
MEM	10uW / 1mW / 35mW	0.3V – 1V power supply for memories
PULP	10uW / 1mW / 35mW	0.3V – 1V power supply for processor

Fig. 1: Overview of the PMU for the wearable medical instrument VivoSoC, which can generate different kinds of power supply for different working modes.

2. SC DC-DC Converter

- Fully integrated on chip
- Compatible with digital SoCs
- Reconfigurable topologies

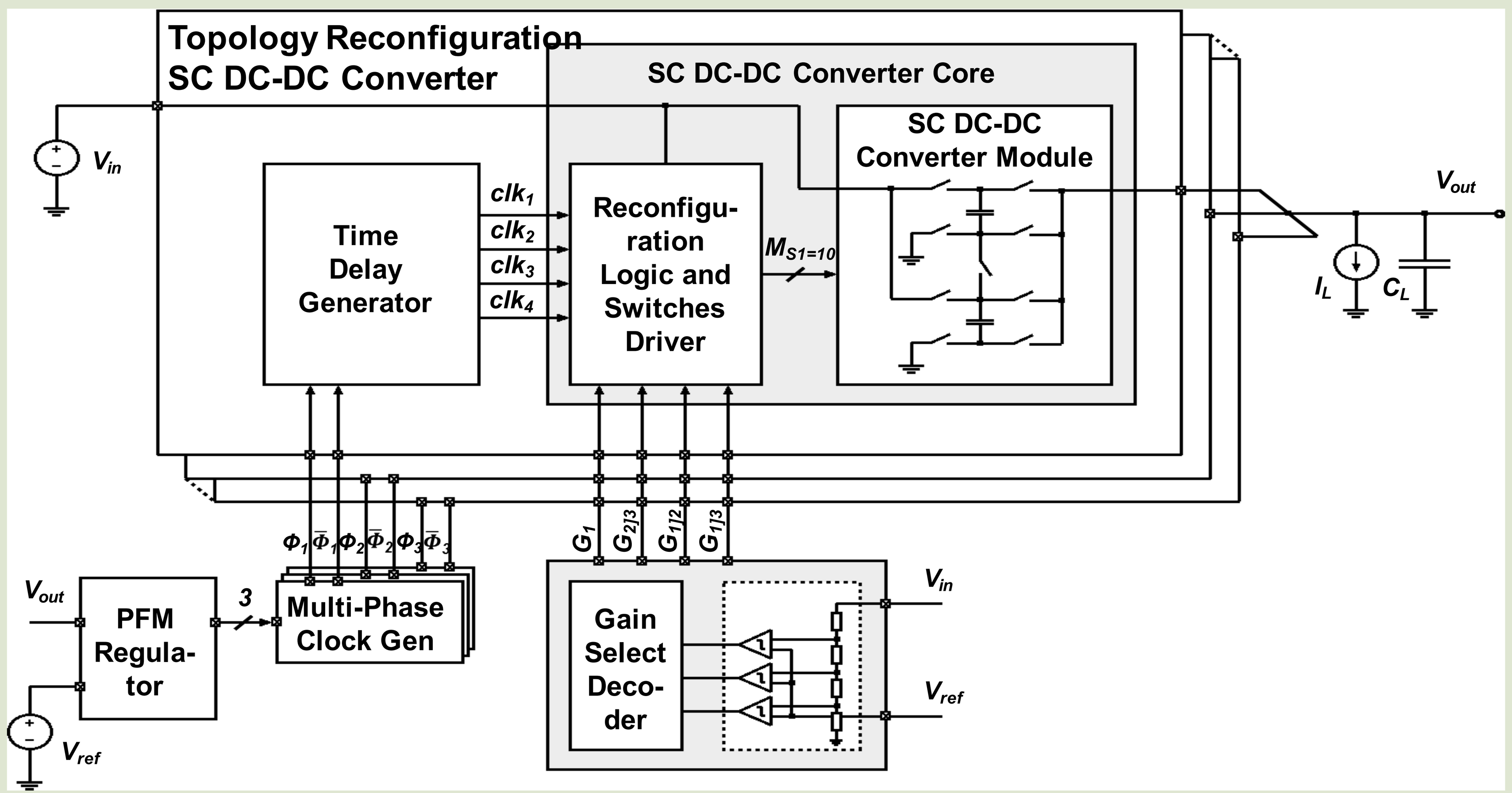


Fig. 2: Top level architecture of the Reconfigurable Switched-Capacitor DC-DC Converter with N fragments

3. Low-Dropout Regulator (LDO)

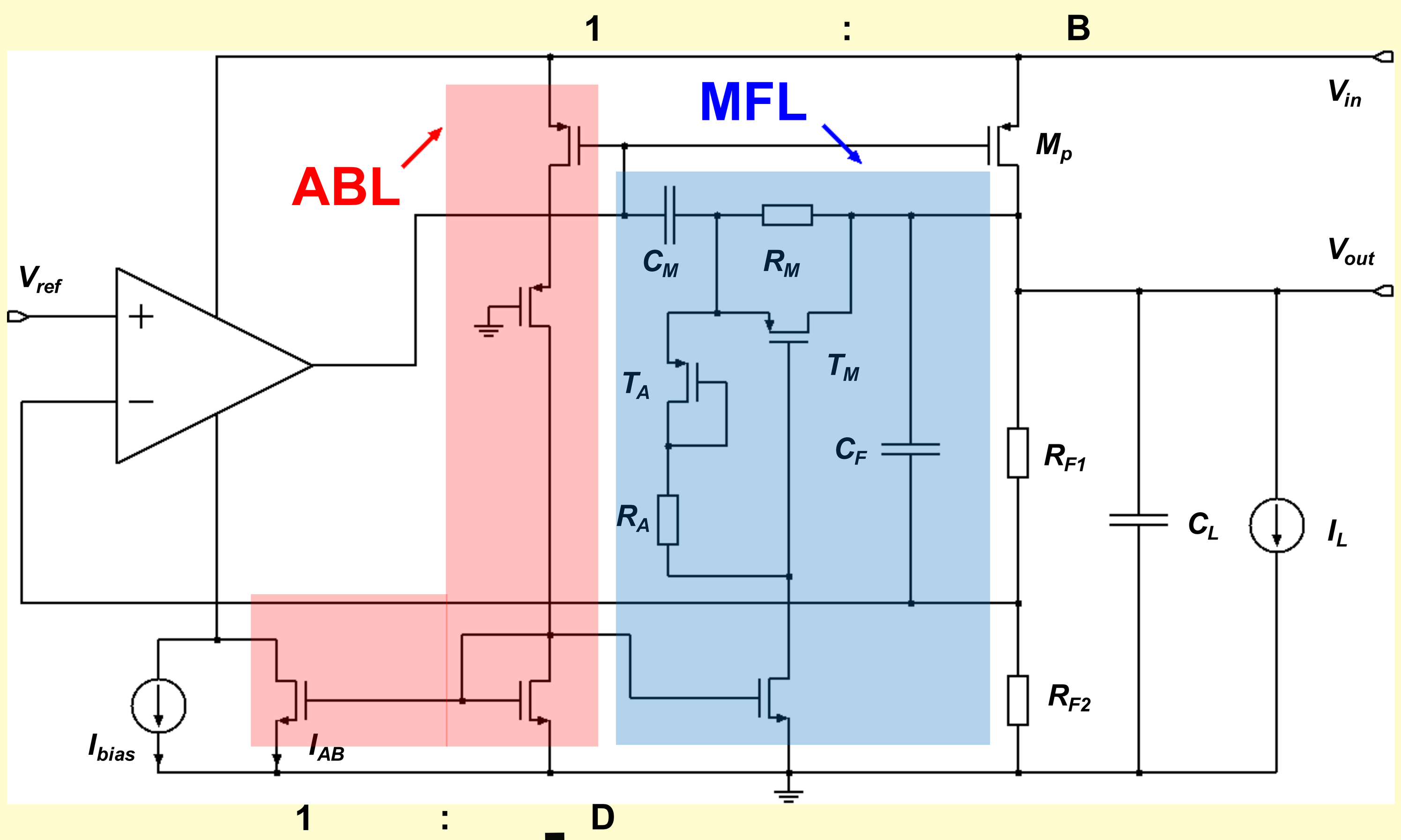
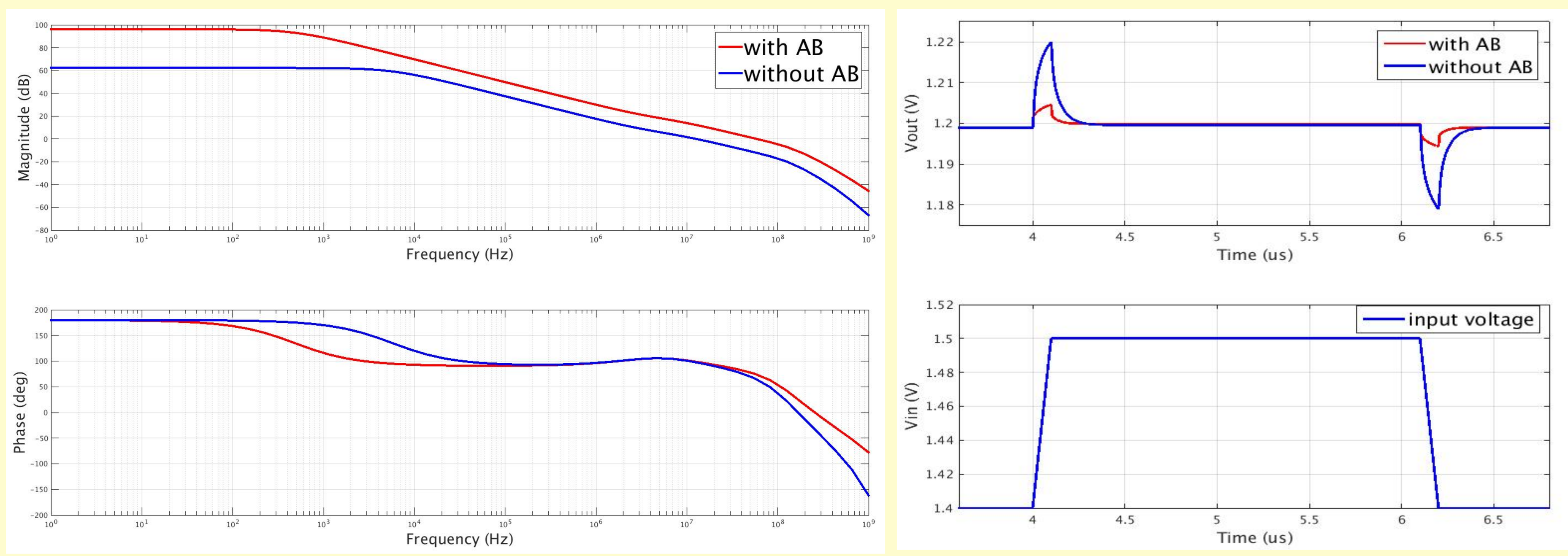


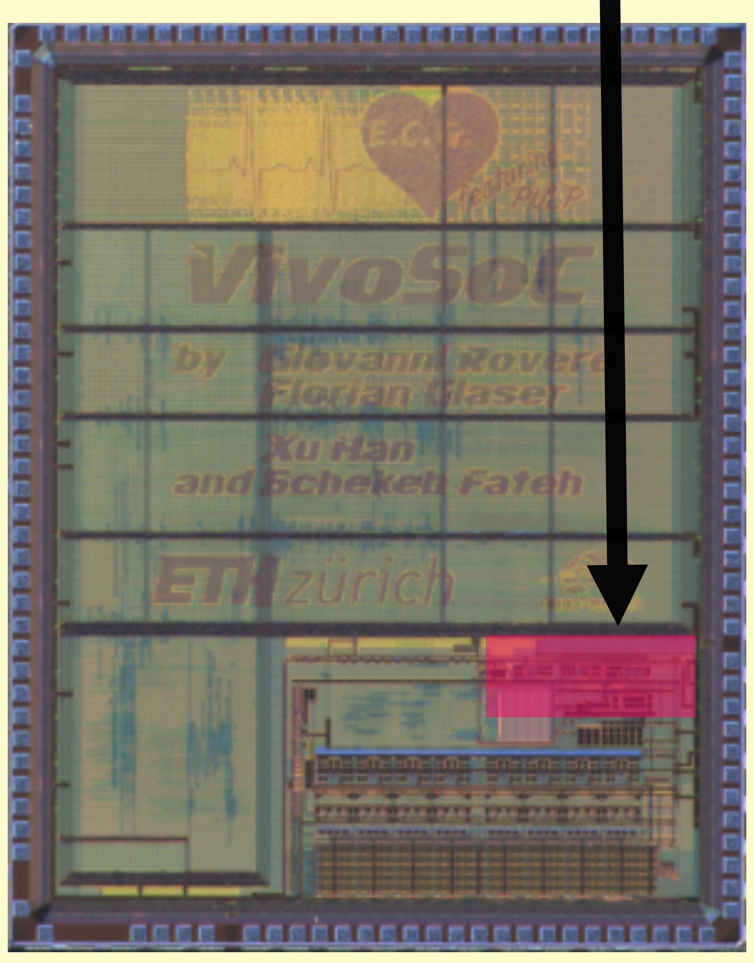
Fig. 3: Schematic of the output-capacitor-free adaptively biased LDO regulator with robust frequency compensation

- LDO consists of two feedback loops: the main feedback loop (MFL) and the adaptive biasing feedback loop (ABL)
- The ABL helps to increase current efficiency and unity gain bandwidth (UGBW)
- The robust frequency compensation network contributes to a better transient response



(a) (b)

Fig. 4: Comparison between regular and the proposed LDO at I_L=10mA (a) open loop frequency response; (b) line regulation transient response



Area	0.048um²
Technology	130nm CMOS
Current Efficiency	82.7% (I_{load}= 100uA) 98.2% (I_{load} = 10mA)
Power Supply Rejection	-45dB (I_{load} = 10mA)
Unity Gain Bandwidth	59MHz (I_{load} = 10mA)

Fig. 5: Chip Layout of the VivoSoC 1 with the LDOs on the chip and measurement results

4. Conclusions and Outlook

Conclusions

- LDO achieves high current efficiency
- The voltage spikes of LDO are reduced during line/load transients

Outlook

- High efficiency Inductor-Based DC-DC Converter with zero current detection
- Fully integrated reconfigurable SC DC-DC Converters to supply Pulp & MEMs

References:

[1] A. P. Chandrakasan, et al. "A 93% Efficiency Reconfigurable Switched-Capacitor DC-DC Converter Using On-Chip Ferroelectric Capacitors," ISSCC, Feb. 2013

[2] W. H. Ki, et al. "Output-Capacitor-Free Adaptively Biased Low-Dropout Regulator for System-on-Chips," TCAS I, May. 2010