nano-tera.ch
swiss scientific initiative in health / security / environment systems

Wearable MRI RTD 2013

FNSNF

ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

University of Zurich[UZH]

An FPGA based real-time data processing platform: Application to real-time coil data compression

Wearable MRI

Josip Marjanovic[1], Jonas Reber[1], David O. Brunner[1], Klaas P. Prüssmann[1]

[1]Institute for Biomedical Engineering, University and ETH Zürich, Zürich

Introduction

Real-time and large-scale computing capabilities are essential prerequisits for the development of new methods in MRI. Especially, fast imaging techniques (e.g., SENSE [1], GRAPPA [2]) rely on data acquisition from a larger number of receive channels simultaneously scaling the demand for computing and data handling. Fast MRI data processing and image reconstruction has already been reported on clusters [3], cloud computers [4] and GPUs [5]. However, many of the numerically costly steps ranging from simple data compression, channel combination or phase extraction up to echo-alignment and frequency correction, could be performed efficiently and with low latency directly on the acquisition system by means of field programmable gate arrays (FPGAs).

Unfortunatelly, the clinical systems are typically not accessible for generic programming, neither equipped with the necessary processing power. Therefore, we deveoped a generic and flexibly programmable real-time processing architecture implemented on a custom spectrometer platform.

The capability of it is demonstrated on the example of noise prewhitening, channel combination and compression in order to reduce the data flow and storage requirements without the requirement of additional CPU load.

Methods

Signal processing architecture

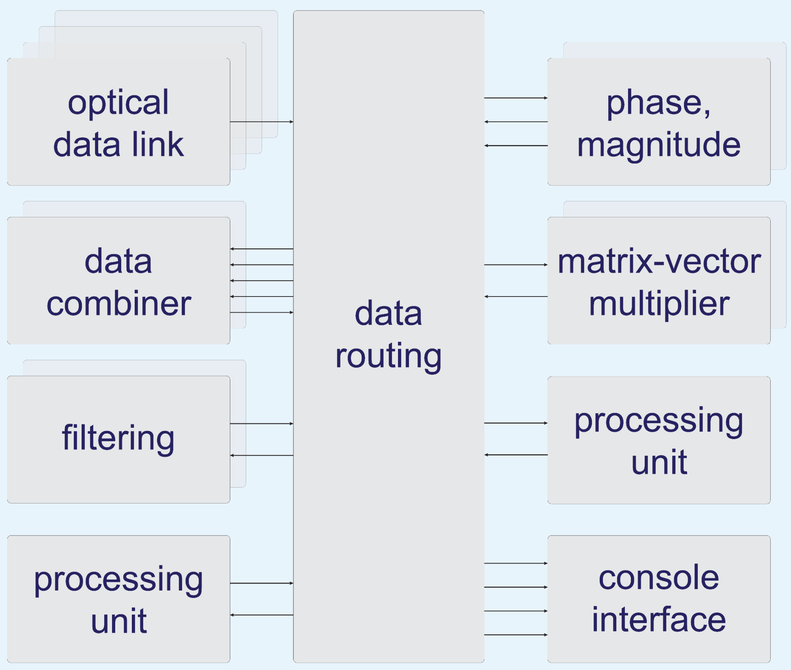
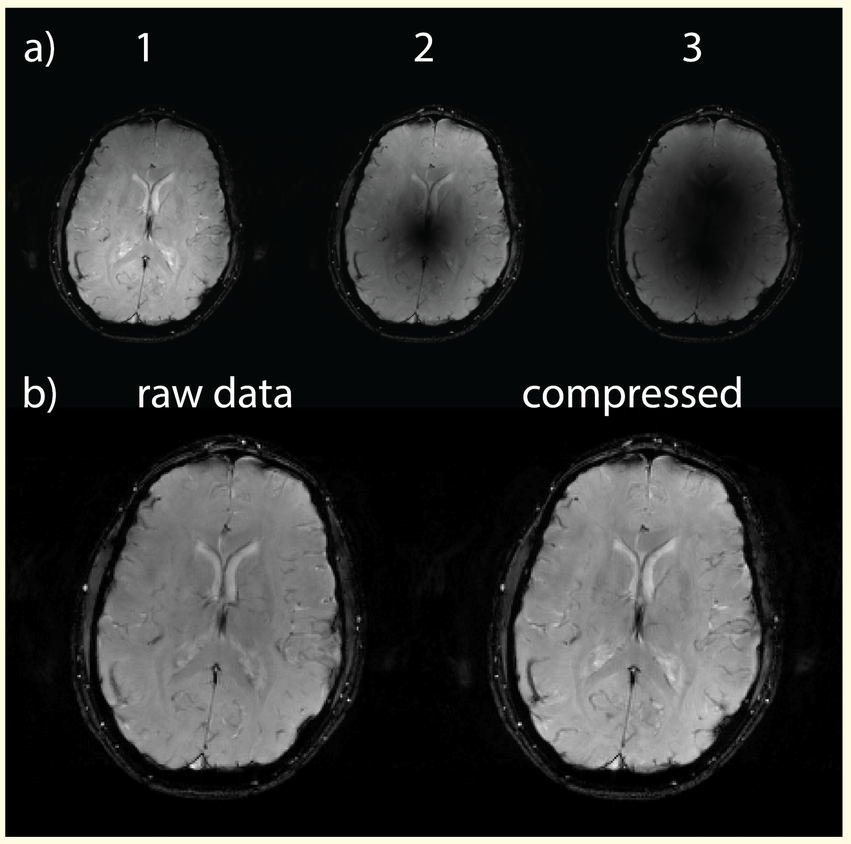


Fig 1. Signal processing architecture: *It is based on generic processing blocks connected to a switching matrix routing the respective data streams. By concatenation of these blocks the numerical task can be flexibly configured. Blocks for phase/amplitude extraction, matrix-vector multiplication and variable-rate filtering were implemented on a custom spectrometer platform based on a Zynq 7 (Xilinx, San Jose, USA) SoC [6]. It has the capability to connect up to four in-field receive modules [7] via high-speed optical lines. The resulting data stream is then handed over to a PXIe system (Nation Instruments, Austin, USA) serving the purpose of a console.*

Coil compression

The data has been acquired using a 3T, 8-channel head coil (Achieva, Philips, Best, The Netherlands). A noise scan and coil sensitivity data were previously acquired and the coil combination and compression coeffitients were calculated by the PCA approach [8] prior to scanning while the channel compression step was performed entirely on the FPGA while scanning.

Results



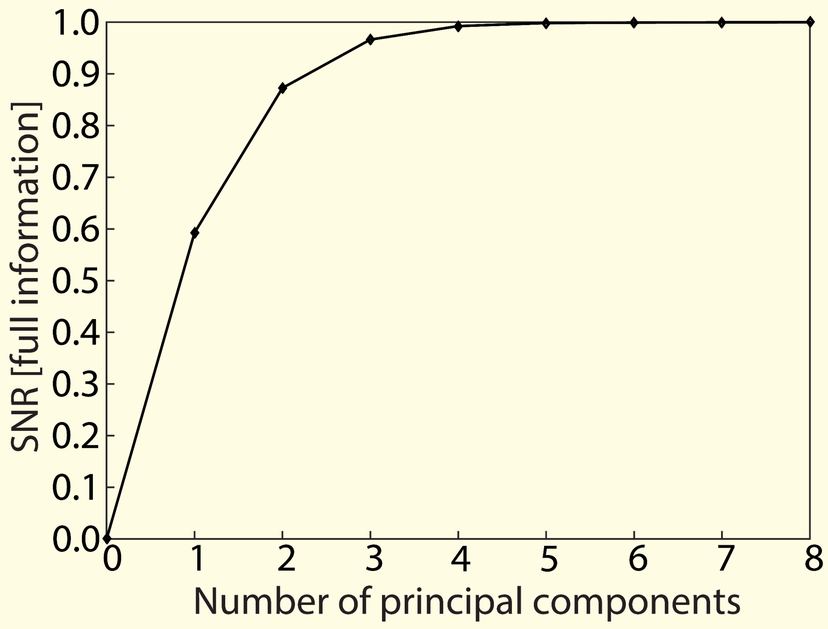


Fig 2. Coil combination experiment - Pricipal components: *A cumulative SNR plot relative to the raw data case in depedence on the number of used eigenmodes. Due to the high correlation of the MRI coils, the first principal component of the 3T 8-channel head coil carries around 60% of the information, the second additional 30%, and the third around 7%.*

Fig 3. Coil combination experiment - in-vivo imaging: a) *The first three virtual coils - principal components of a human head image acquired using a 3T 8-channel head coil. As expected the first principalvirtual coil carries most of the information, while the other two carry information only on the border where the coils correlate less emphasizing the need for further principal components to faithfully reconstruct the image.* ***b)*** *A comparison of an image reconstructed using all 8 raw data channels and the three most significant virtual coils. As the last carry more than 97% of the information differences can't be hardly observed by naked eye.*

Discussion

The proposed FPGA architecture allows implementening high-throughput processing units which can perform highly paralellized and low latency computing tasks in custom configured pipelines. Frequently encountered bottlenecks such as back planes, ethernet links and mass storage drivers can be successfully avoided. Further reconstruction steps can be performed on CPUs focusing on the more complex tasks such as gridding without significantly reduced numerical burden.

References

(1) Pruessmann KP et al. MRM 1999;42:952
(2) Griswold MA, MRM 2002;47:1202
(3) Borisch E et al. Procs. ISMRM 2008
(4) Xue H, MRM 2015; 73:1015
(5) Stone S. et.al, J Parallel Distrib Comput 2011
(6) Reber J, Procs. ISMRM 2016
(7) Reber J, Procs. ISMRM 2014
(8) Buehrer M et al., MRM 2007; 57:1131