nano-tera.ch
swiss scientific initiative in health / security / environment systems

WearableMRI RTD 2013

FNSNF

Integrated Receiver and Synchronization IC for Wearable MRI

ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

B. Sporrer, L. Wu, L. Bettini, T. Burger, Q. Huang

Integrated Systems Laboratory – ETH Zurich

Wearable MRI

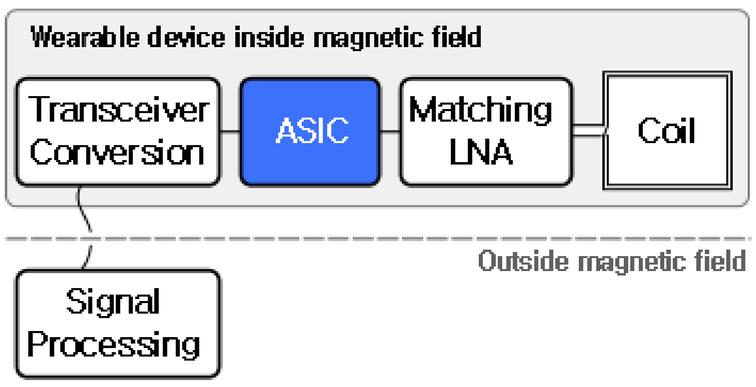


Fig. 1: System overview of the wearable MRI implementation.

- ❑ **Small area**
  Reducing distortion of large in-bore magnetic fields to the receiver
- ❑ **Minimum noise figure**
  Additional receiver noise increases required scan time
- ❑ **Large dynamic range**
  Input signal levels from noise floor up to 74dB SNR encountered
- ❑ **High decoupling between coils**
  Avoiding noise coupling between channels
- ❑ **Low Power**
  Allows use of non-galvanic power distribution

1 Motivation & Requirements

- ❑ **2 full receive chains on chip**
- ❑ **Total receiver noise figure below 2dB**
- ❑ **High dynamic range exceeding 74dB of SNR**
- ❑ **Adjustable gain allows to adopt to peak input level of every scan**

- ❑ **Configurability in input impedance, receive frequency and gain distribution allow the use of the receiver in multiple applications**
- ➢ **The high upfront cost of integration is spread over multiple products**

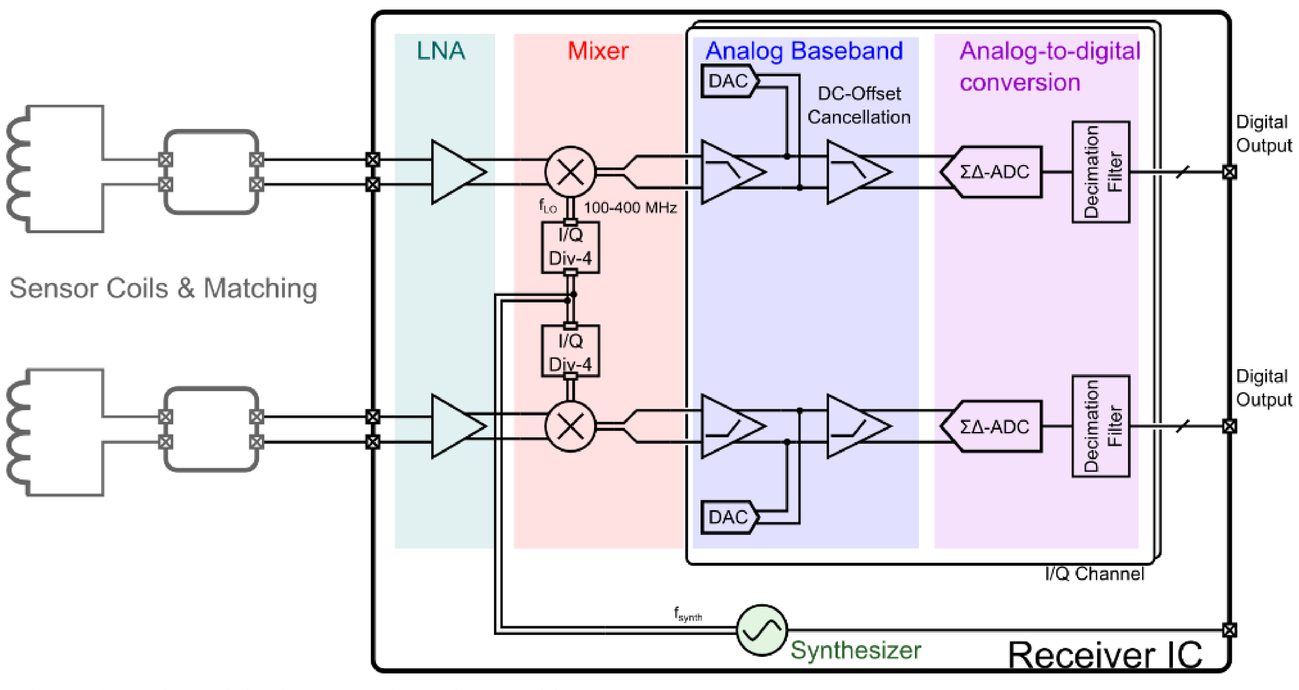
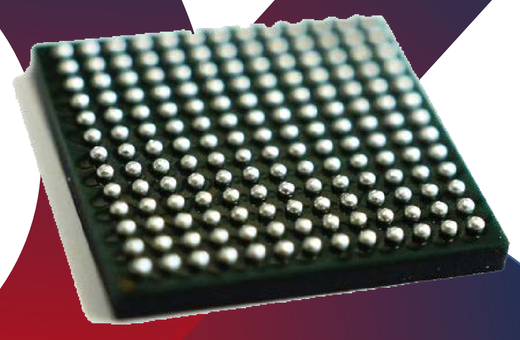


Fig. 2: Overview of the integrated receiver architecture.

2 Receiver Integration



3 Clock Generation

- ❑ **High quality system clock and on-board crystal oscillator available as clocking solution**
- ❑ **Generated LO is sent to the MRI system to allow for post-correction of the image**
- ❑ **Low-jitter narrow-bandwidth charge-pump PLL assisted by harmonic enhanced VCO to achieve higher maximum SNR at high input frequencies**

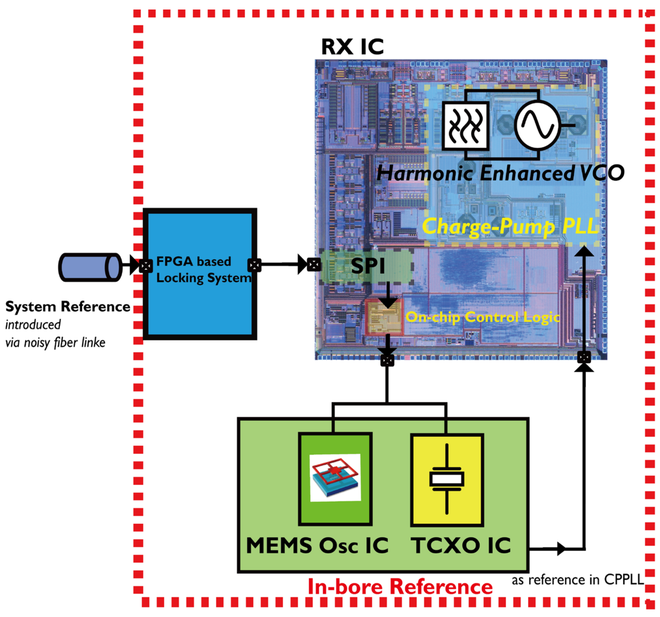


Fig. 3: Proposed In-bore Clocking System.

4 Results

Field strength	1.5T - 7T
Frequencies	64-300MHz
Gain	20…64 dB
Power	350 mW (1.5/2.9 V)
Chip-area	15 mm^2
Package-area	49 mm^2

Fig. 4: Performance of the receiver IC

- ❑ **Required performance for 3T/7T imaging reached, comparable to state-of-the-art rigid arrays**
- ❑ **Full receiver chain on 15mm^2 of silicon area, 49mm^2 total area of package, drastically decreasing board size**
- ❑ **Power consumption well below 1W per channel allows safe operation near patient**
- ❑ **Chip operation verified inside the MRI bore. Circuitry withstands high gradient/RF fields**

References:
[1] B. Dietrich, et al. “A stand-alone system for concurrent gradient and RF sequence monitoring,” ISMRM 2012: 700.
[2] N. De Zanche, et al. "Modular design of receiver coil arrays," NMR in Biomedicine 21.6 (2008): 644-654.
[3] J. Rogin, et al. "A 1.5-V 45-mW direct-conversion WCDMA receiver IC in 0.13-µm CMOS," Solid-State Circuits, IEEE J. Solid-State Circuits, vol. 4, no. 12, pp. 2239-2248, Dec. 2003.
[4] B. Sporrer, et al. "Integrated CMOS receiver for wearable coil arrays in MRI applications," *Design, Automation & Test in Europe (DATE), 2015* , pp.1689,1694, 9-13 March 2015