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BOLT: A Stateful Processor Interconnect

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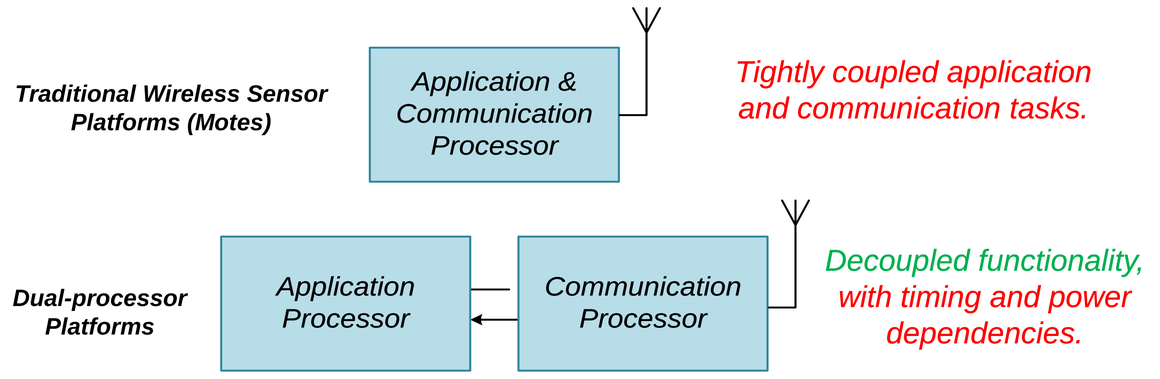
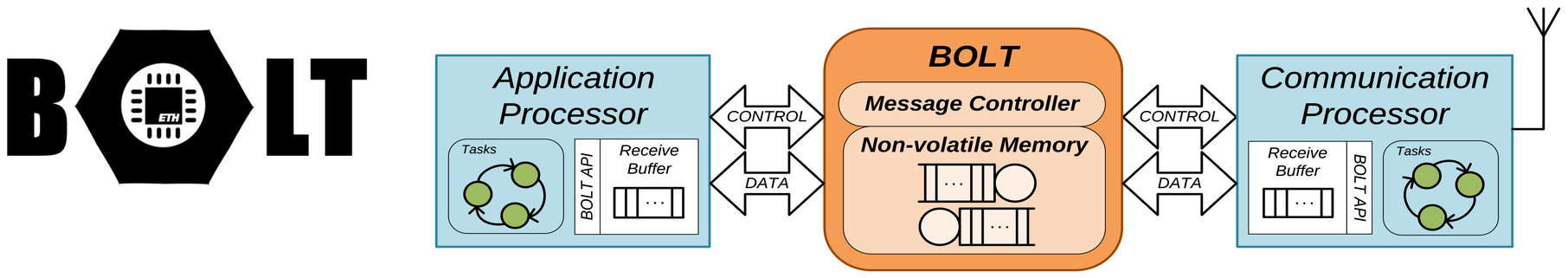
> Motivation

- *Traditional wireless sensor platforms enabled initial simple sense-and-send applications, e.g. environmental monitoring, on a single processor.*
- *In today's distributed embedded system landscape, the ever **increasing resource demands** and the requirements for **run-time adaptability** and **low power consumption** encourage the adoption of **multi-processor** architectures.*
- *However**, interference on shared resources**, e.g., peripherals and memory, seriously hampers modularity, predictability and energy-proportional system performance.*



> Interconnect Architecture



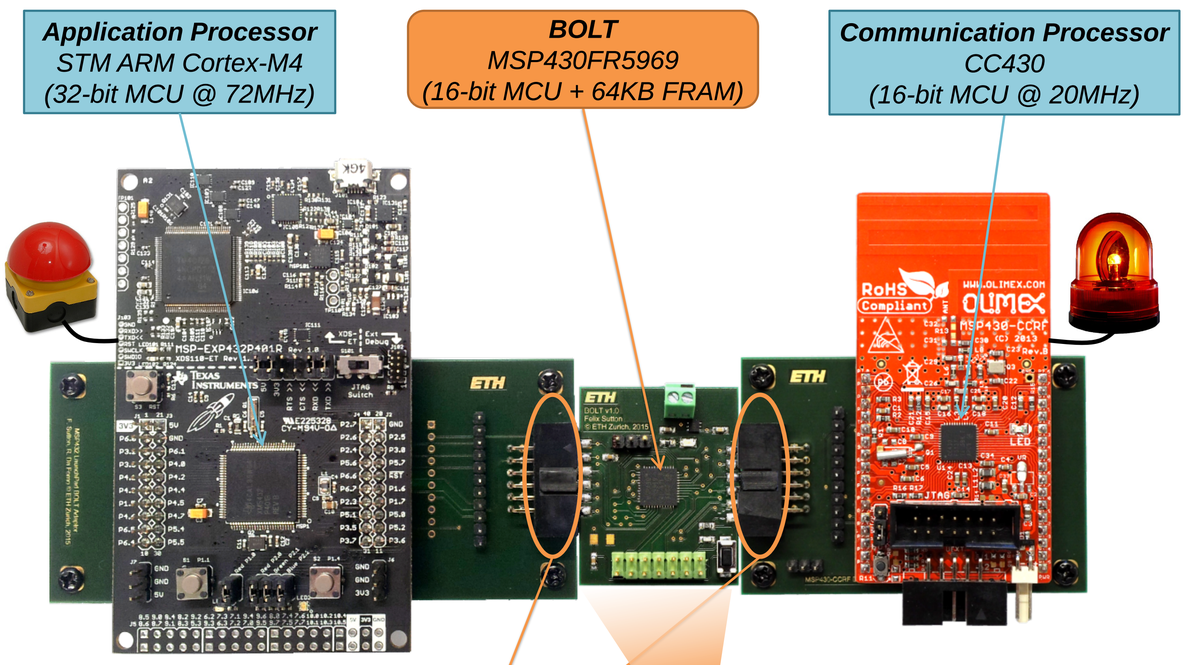
*Decoupled application and communication tasks with respect to **time, power and clock.***

***BOLT** is the first processor interconnect that allows any two arbitrary processors to execute within their **own time, power and clock domains**, while supporting **predictable inter-processor communication** through asynchronous message passing.*

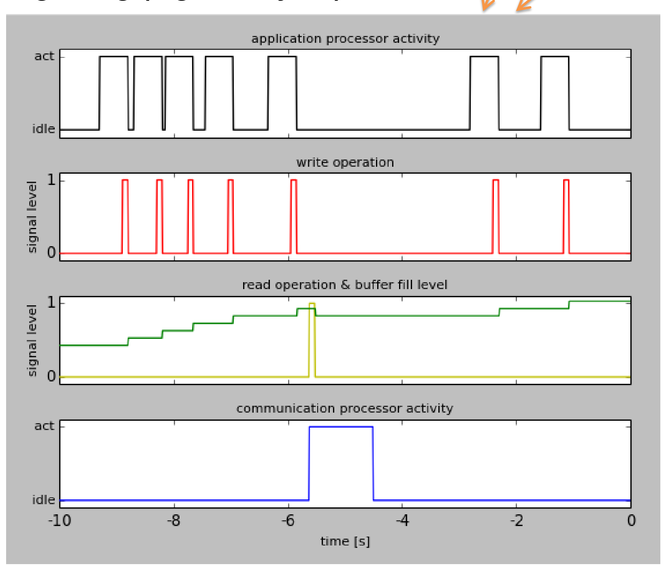
- ✓ ***Avoidance of resource interference***
- ✓ ***Tight bounding of unavoidable interference***
- ✓ ***Formal specification of communication interface***

*Paradigm shift towards **compositional** construction and **predictable** operation of heterogeneous **ultra low-power** wireless sensor platforms.*

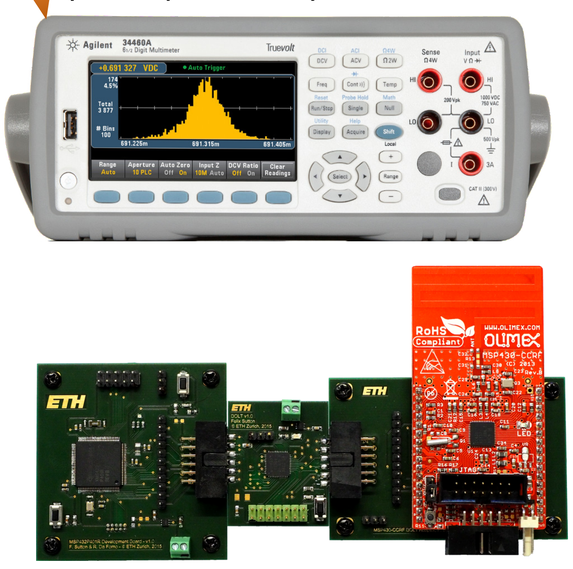
> Prototype Evaluation and Demonstration



signaling (logic analyzer)



power (multimeter)



BOLT in Action:

A wireless sensing application obliged to react to asynchronous sensor events on the application processor, and periodic network events on the communication processor:

(1) A sensor event is generated by pushing a button.
(2) An interrupt on the application processor (A) triggers a wake-up from deep sleep mode. After processing the sensor event, an alarm message is written to BOLT and A goes back to sleep mode.
(3) As soon as the message has been successfully written to BOLT, the IND line is asserted to notify the communication processor (C) of the pending message.
(4) Processor C is duty-cycled and participates in periodic network communication. It only reads at most one message from BOLT before each communication round and indicates this with a flashing lamp.

Power Analysis:

- *Ultra-low **1.2µW** @ **3.0V** power dissipation of BOLT in idle mode.*
- *Non-excessive **1.1mW** @ **3.0V** power dissipation during message operations.*
- *Elaborate application and communication processor selections will lead to optimal energy efficiency while sustaining reactivity.*